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**All-optical Router with PPM Header  
Processing in High Speed Photonic  
Packet Switching Networks**

**Hoa Le Minh**

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of Northumbria University for the degree of  
Doctor of Philosophy

Research undertaken in the School of  
Computing, Engineering and Information Sciences

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## ABSTRACT

Rapidly growing internet traffic volume is the major driving force behind the development of optically-transparent and ultrahigh-capacity photonic packet-switching networks. In such networks, the packet routing decision at each router is made by sequentially correlating an incoming packet header address with addresses in all entries of the router's look-up routing table. The routing task is achieved in the optical domain using all-optical logic gates and optical correlator technologies which have been predominantly replacing the existing low-speed electronic processing devices. Nevertheless when a network is expanded, a larger routing table is required thus exponentially increasing header processing time, which results in the increases in routing latency and complexity.

This research aims to significantly reduce the size of the routing table and the number of optical devices required in a router by mapping both the packet header address and the look-up routing table entries into the pulse-position-modulation format, where more than one address could be located in a single entry of a new pulse-position routing table. By simply carrying out a single correlation of the packet header address with pulse-position routing table entries, the router can instantly obtain the routing decision, thus significantly reducing the processing time and neglecting the gain recovery time in existing optical logic gates. The structure of the pulse-position routing table also offers flexibility in the transmission mode including unicast, multicast or broadcast embedded in the optical (physical) layer. In the thesis, a new router based on the pulse-position-modulation scheme will be introduced. Essential router modules including high on-off

contrast-ratio clock extraction, pulse position routing table, header processing and optical switch are proposed and analysed. In addition, the thesis investigates and improves the switching window profile and residual crosstalk performance of the all-optical Mach-Zehnder switches as a building block for the implementation of the above router modules. A number of new variants of Mach-Zehnder-based switches are also introduced to enhance switching inter-output contrast ratio and reduce the complexity in multiple-channel OTDM demultiplexing.



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Finally, to my beloved parents and my dear wife Hong Van, I express my utmost gratitude and thanks, for without them, I would have never made it this far.

## **DECLARATION**

I hereby declare that this thesis is entirely my own work and has not been submitted in support of an application of another degree or qualification of this or any other university, institute of learning or industrial organisation

Signature:

Name: Hoa Le Minh

Date: 09 May 2007

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## **GLOSSARY OF ACRONYMS**

2R.....	Reshaping and Re-amplification
3R .....	Reshaping, Retiming and Re-amplification
AOFF .....	All-Optical Flip-Flop
AOLS .....	All-Optical Label Switching
ASE.....	Amplified Spontaneous Emission
AWG.....	Arrayed Waveguide Grating
B2B .....	Back-to-Back
BER.....	Bit Error Rate
BERT .....	Bit Error Rate Tester
CEM.....	Clock Extraction Module
CSMZ.....	Chained Symmetric Mach Zehnder
CCW .....	Counter Clockwise
CP.....	Control Pulse
CR .....	On/off Contrast Ratio
CXT .....	Crosstalk
CW .....	Clockwise
DCF.....	Dispersion Compensation Fibre
DWDM .....	Dense Wavelength Division Multiplexing
EAM.....	Electro Absorption Modulator
EC .....	Eye Closure
EDFA .....	Erbium-Doped Fibre Amplifier

FBL .....Feedback Loop  
 FEC .....Forwarded Error Control  
 FWHM .....Full Width Half Magnitude  
 FWM .....Four Wave Mixing  
 MEMS .....Micro-Electro-Mechanical Systems  
 MPLS .....Multi-Protocol Label Switching  
 MW-PPRT .....Multi-Wave Pulse Position Routing Table  
 MZI .....Mach-Zehnder Interferometer  
 NF .....Noise Figure  
 NOLM .....Nonlinear Optical Loop Mirror  
 NRZ .....Non-Return to Zero  
 IC .....Integrated Circuit  
 IP .....Internet Protocol  
 ISI .....Inter-Symbol Interference  
 IT .....Informatics Technology  
 IVR .....Intensity Variation Ratio  
 OADM .....Optical Add/Drop Multiplexer  
 OBS .....Optical Burst Switching  
 OCS .....Optical Circuit Switching  
 O-E-O .....Optical-to-Electrical-to-Optical  
 OLS .....Optical Label Switching  
 OPS .....Optical Packet Switching  
 OSW .....Optical Switch



OSWC.....	Optical Switch Controller
OSNR.....	Optical Signal-to-Noise Ratio
OTDM.....	Optical Time Division Multiplexing
OXC.....	Optical Cross-Connect
PBS .....	Polarisation Beam Splitter
PC.....	Polarisation Controller
PIN.....	P-type Intrinsic N-type diode (a diode with a wide, undoped intrinsic semiconductor region between p-type semiconductor and n-type semiconductor regions)
PPM .....	Pulse Position Modulation
PPM-ACM.....	Pulse-Position-Modulation Address Conversion Module
PPM-HP.....	Pulse Position Modulation Header Processing
PPRT.....	Pulse Position Routing Table
PRBS.....	Pseudo Random Bit Sequence
PSPC .....	Photonic Serial-to-Parallel Converter
RCXT.....	Residual Crosstalk
RIN.....	Relative Intensity Noise
RMS .....	Root Mean Square
RT .....	Routing Table
RZ .....	Return to Zero
SCM.....	Sub-Carrier Modulation
SDH .....	Synchronous Digital Hierarchy
SESHG.....	Surface-Emitted Second-Harmonic Generation

SMZ .....Symmetric Mach Zehnder  
 SOA .....Semiconductor Optical Amplifier  
 SONET.....Synchronised Optical Network  
 SPM .....Self Phase Modulation  
 SSMF .....Standard Single Mode Fibre  
 SW .....Switching Window  
 TaMZ .....Tri-arm Mach Zehnder  
 TOAD .....Terahertz Optical Asymmetric Demultiplexer  
 UF-OSW .....Ultrafast Optical Switch  
 UNI .....Ultrafast-Nonlinear Interferometer  
 VPI.....Virtual Photonics Inc.  
 WC .....Wavelength Converter  
 WDM .....Wavelength Division Multiplexing  
 XGM .....Cross Gain Modulation  
 XPM.....Cross Phase Modulation

## GLOSSARY OF SYMBOLS

$\alpha$ .....	Coupling ratio
$\alpha_{\text{LEF}}$ .....	Linewidth enhancement factor
$a$ .....	Signal field gain
$a_i$ .....	The $i^{\text{th}}$ bit in the packet header address
$a_{\text{PPM}}$ .....	Converted PPM address
$A$ .....	SOA surface and defect recombination coefficient
$A_{\text{SOA}}$ .....	Cross-section area of active region
$\beta$ .....	Combination factor of CP <sub>1</sub> in TaMZ
$B$ .....	SOA radiative recombination coefficient
$B_e$ .....	Electrical bandwidth
$B_o$ .....	Optical bandwidth
$C$ .....	SOA auger recombination coefficient
$CXT$ .....	Crosstalk
$CXT_{\text{D-CP}}$ .....	Data-control crosstalk
$\delta$ .....	Splitter factor to feedback power to the FBL in AOFF
$\Delta\phi$ .....	Phase difference between two gain profiles
$\Delta\phi_{\text{pol}}$ .....	Polarisation phase difference between two signals
$\Delta P_{\text{rx}}$ .....	Received power penalty
$E_e$ .....	Electron energy
$E_m$ .....	PPRT entry $m$

$f_0$ .....	Optical signal frequency
$g$ .....	Gain coefficient
$g_d$ .....	Differential gain (gain per unit length)
$G(t)$ .....	Gain profile
$G_0$ .....	Unsaturated amplifier gain
$G_{CCW}$ .....	Counter-clockwise semiconductor-optical-amplifier gain profile
$G_{CP}$ .....	Gain of control pulse in the clock extraction module
$G_{CW}$ .....	Clockwise semiconductor-optical-amplifier gain profile
$G_{OSW}$ .....	Optical switch gain
$G_{SOA}$ .....	SOA gain
$\Gamma$ .....	Confinement factor of SOA
$K$ .....	Total number of PPRTs in PPM-HP scheme employing multiple PPRTs
$I_{0d}$ .....	Distorted bit “0” intensity
$I_{0u}$ .....	Undistorted bit “0” intensity
$I_{1d}$ .....	Distorted bit “1” intensity
$I_{1u}$ .....	Undistorted bit “1” intensity
$I_{ASE}$ .....	Equivalent amplified spontaneous emission current
$i_a^2$ .....	Power spectral density of the electrical amplifier input noise current
$I_e$ .....	Effective DC injection current
$\bar{I}_m$ .....	Received mean photocurrent for the received mark signal
$\bar{I}_s$ .....	Received mean photocurrent for the received space signal
$\kappa$ .....	Input splitting factor (in PPM-HP router)
$\lambda$ .....	Optical signal wavelength

$L$ .....	Number of delay stages in multiple-pulse generation of OSWC
$L_{\text{excess}}$ .....	Excess loss of the coupler/splitter
$L_f$ .....	Optical filter loss
$L_{\text{PPRT}}$ .....	Total power loss due to PPRT
$L_{\text{S/R}}$ .....	Number of pulses in <b>S</b> or <b>R</b> signals of AOFF
$L_{\text{SOA}}$ .....	SOA length
$M$ .....	Total number of PPM-HP router outputs
$m_A$ .....	Decimal metric of the binary-formatted address bits
$mch$ .....	Matching pulse
$n$ .....	Refractive index
$N$ .....	Number of bits in packet header address
$N(t)$ .....	Carrier density
$N_m$ .....	Number of pulses in an entry $E_m$ (i.e. number of the $\mathbf{P}_m$ elements)
$N_{m,\text{tot}}$ .....	Total entries in a routing table
$n_{\text{sp}}$ .....	Optical amplifier inversion parameter
$N_T$ .....	Carrier density at transparency
$N_{\text{tot}}(t)$ .....	Total carrier of SOA
$\eta_{\text{in}}$ .....	SOA input coupling efficiency
$\eta_{\text{out}}$ .....	SOA output coupling efficiency
$N_{\text{PPM-HEM}}$ .....	Number of generated pulses at the PPM-HEM output
$NF_0$ .....	Preamplifier noise figure
$NF_{\text{SOA}}$ .....	SOA noise figure
$NF_{\text{OSW}}$ .....	OSW noise figure

$p(t)$ .....	Input optical pulse
$P$ .....	Optical power
$P_{CCW}$ .....	Optical power of counter-clockwise component
$P_{CP}$ .....	Control pulse peak power (for OSW)
$P_{CP-X}$ .....	Control pulse peak power projected to X-polarisation (for OSW)
$P_{CP1}$ .....	Control pulse peak power (control pulse 1)
$P_{CP2}$ .....	Control pulse peak power (control pulse 2)
$P_{CS-in}$ .....	Peak power of input pulse applied to the delay groups in optical switch
$P_{CS-out}$ .....	Peak power of output pulse from the delay groups in optical switch
$P_{CW}$ .....	Optical power of clockwise component
$P_e$ .....	Peak power of $e(t)$ pulse input to PPRT
$P_{FBL}$ .....	Average power in AOFF feedback loop
$P_{in-t}$ .....	Total input power
$\mathbf{P}_m$ .....	Set of the decimal metrics of address patterns having the same output port #m
$P_{nt}$ .....	Power of switched non-target signal
$P_{rx}$ .....	Average received power
$P_{pk}$ .....	Packet (pulse peak) power
$P_{pk-sw}$ .....	Packet (pulse peak) power applied to the individual switch of OSW
$P_s$ .....	Average received signal (single pulse or data packet) power without $RCXT$
$P_{R,avg}$ .....	Average power of control pulses in <b>R</b> stream
$P_{S,avg}$ .....	Average power of control pulses in <b>S</b> stream

$P_{\text{SMZ1}}$ .....	Power of control pulse applied to 1×2 two-SMZ based switch ( $CP_{\text{SMZ1}}$ )
$P_t$ .....	Power of switched target signal
$P_{\text{out-t}}$ .....	Total output power
$\rho_e$ .....	Electron density
$R$ .....	Reduction (power) ratio
$RCXT$ .....	Residual crosstalk
$RCXT_{\text{opt}}$ .....	Residual crosstalk determined at $R_{\text{opt}}$
$R_L$ .....	Load resistance of photodetector
$R_{\text{opt}}$ .....	Optimum reduction (power) ratio
$R_p$ .....	Photodetector responsivity
$R_{\text{sp}}$ .....	SOA recombination rate
$R_T$ .....	Header recognition time gain
$\text{RIN}_T$ .....	Relative intensity noise of transmitter
$\text{RIN}_{\text{TOAD}}$ .....	Relative intensity noise of TOAD
$\text{RMS}_{\text{RIN-TOAD}}$ .....	Relative intensity noise variance of TOAD
$\text{RMS}_{\text{RIN-SMZ}}$ .....	Relative intensity noise variance of SMZ
$r$ .....	Switching extinction ratio
$\sigma_{\text{receiver}}^2$ .....	Receiver noise power
$\sigma_{\text{RIN}}^2$ .....	Relative intensity noise power
$\sigma_{\text{SOA}}^2$ .....	ASE noise power of SOA
$\sigma_{t,m}^2$ .....	Total noise power in the received mark signal
$\sigma_{t,s}^2$ .....	Total noise power in the received space signal

$T_{ACM}$ .....	Delay required for inputting $CP_{PPM-ACM}$ to PPM-ACM
$T_{AND}$ .....	Time required for gain recovery in an all-optical AND gate
$T_b$ .....	Bit duration
$T_{CEM}$ .....	Time required for clock extraction in CEM
$T_{CP-HEM}$ .....	Duration of control signal for HEM
$T_{EX-HP}$ .....	Processing time required for exhaustive correlation
$T_{FBL}$ .....	Delay associated with a feedback loop
$T_k$ .....	Temperature (in Kelvin degree)
$T_{int}$ .....	Switching interval
$T_{pk}$ .....	Packet duration
$T_{PPM-HP}$ .....	Processing time required for PPH-HP module
$T_{PPRT}$ .....	Delay required for inputting $e(t)$ to PPRT
$t_{sampling}$ .....	Sampling time (eye pattern)
$T_{SOA}$ .....	Time for signal propagating through a SOA
$T_{sp}$ .....	SOA spontaneous emission time (carrier lifetime)
$T_{SW}$ .....	Switching window width
$T_s$ .....	PPM slot time
$V_g$ .....	Group propagation velocity
$V_{SOA}$ .....	Active volume of SOA
$h$ .....	Planck constant ( $6.6260693 \times 10^{-34}$ J.s)
$k$ .....	Boltzmann constant ( $1.3806505 \times 10^{-23}$ J/K)
$q$ .....	Electron charge ( $1.60217653 \times 10^{-19}$ C)



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# CHAPTER 1

## INTRODUCTION

### 1.1 Research Fundamentals

Nowadays, the rapid increase in the volume of the internet traffic is one of the major driving forces for the ever growing needs of all-optical-based communication systems that offer a much greater transmission bandwidth, higher end-to-end reliability and cheaper installation cost compared to the copper-wire, optoelectronic-based and satellite communication systems in long-haul transmissions. Optical fibre communication networks were first introduced with a simple topology of point-to-point connection, which did not require address recognition nor packet routing capabilities. In these optical systems high transmission capacity is achieved by employing *wavelength division multiplexing* (WDM) and *optical time division multiplexed* (OTDM) techniques [1, 2] where a number of channels in different wavelengths and different time-slots, respectively, are transmitted along a single fibre. Second-generation optical networks such as *synchronous optical network* (SONET) and *synchronous digital hierarchy* (SDH) schemes were developed [3] offering additional features such as packet processing, switching and routing in complex network topologies including star, ring and mesh. Nevertheless, in such networks, the main processing and switching actions at



intermediate routers are performed in the electrical domain, requiring extensive use of optical-to-electrical-to-optical (O-E-O) conversion modules [4]. In the ultrafast dense-WDM (DWDM) [5, 6] and OTDM [7, 8] networks, where the aggregate bit rate exceeds 100 Gbit/s, O-E-O modules are not only costly, but also impose the speed bottleneck beyond 40 Gbit/s owing to the limitations of processing speeds and the response of the electronic devices [9-11]. As a result, the aggregate switching throughput of an optical network depends on the processing and switching speed at individual nodes/routers within the network. Therefore, future truly ultrafast photonic networks must be optically transparent which implies that data packets are processed and routed inside the network, regardless of bit rates and protocols, without being converted into the electrical domain at intermediate routers.

In recent years, we have seen comprehensive research activities in development of packet switching routers in the optical domain for ultrahigh-capacity photonic DWDM and OTDM networks [12-24]. Although the tasks for designing all-optical routers are substantial and complex, it is possible to carry out routing in optical domain owing to the rapid progress in the development of ultrafast optical switches (UF-OSW) [9, 11, 25] based on the *semiconductor optical amplifier* (SOA) [26-32]. In all-optical router a SOA is the crucial component for realising key all-optical functions such as all-optical packet synchronisation, optical signal processing (header recognition, wavelength conversion, 2R, 3R, equalization, etc.) and packet switching [33-40]. Additionally, the UF-OSW employing a SOA offers integration capability and typically consumes low optical energy ( $\sim$  pJ) [9, 11, 37, 41]. Among the main elements of a router, header recognition

is the most challenging task owing to the enormous hardware requirements for optical implementation of correlations between packet header address and a large number of look-up routing table (RT) entries, which contain information for making a routing decision. A number of all-optical header recognition approaches have been proposed, requiring a range from simple to robust optical processing mechanisms. The simplest router's header recognition is configured by the all-optical self-driven packet switching scheme where the look-up routing table is known in advance at the source router. The packet address conveys a set of bits to switch on/off the states of individual intermediate core router's optical switches [17, 21, 42] for the packet being switched to the next hop. Although this scheme is attractive for small scale all-optical routing, however it is not suitable for a large scale network consisting of many intermediate routers/nodes because of the increase in header length requirement for multiple-hop routing. Partial header recognition employed in the optical bypass router has been proposed in [16, 43] offering a partially optical solution for routing in large scale networks. The router optically processes only a small subset in the packet header addresses which have a high probability in selection of a specific routing path [16]. The optical header recognition utilises a bank of all-optical mirror-based correlators and a threshold detector for optical correlations. The remaining packets with addresses excluded from this subset are processed in the main electronic router which will in turn introduce additional speed-bottleneck latency for those packets. The bypass router offers higher aggregate transmission throughput in comparison to a conventional electrical router, but not all packets are optically processed. Recently, the emerging multi-protocol label-swapping-based (MPLS) router has been proposed in [13, 15, 22, 44-49] to provide ultrafast

optical packet-switching transparency by attaching an additional lower bit rate optical label at a wavelength different from the packet wavelength for conveying destination address information. The label is correlated with the intermediate router's address patterns stored in a built-in look-up routing table. Therefore it provides complete optical transparency for packet switching, at the same time keeping a short label length. Nevertheless, in this router, all-optical logic gates are employed for header address recognition using an exhaustive (brute-force) correlation algorithm, i.e. checking all possible address patterns for making routing decisions, which therefore requires highly complex hardware implementations. In addition it introduces a large processing delay due to two main issues: (i) an exponential increase in the number of routing table entries due to a long packet header address and (ii) a slow response-time of the all-optical logic gates employing SOA because of a long SOA gain recovery time (i.e. SOA carrier density relaxing time). In a larger-size core network, where the size of the look-up routing table at the core router is large (i.e. few-hundred entries), the router's scalability is limited due to its architecture complexity and its associated cost (optical devices). Although these issues have continuously been improved with the penetration of the optical technology into the telecommunications market, it is still too costly to put together a large-scale all-optical packet switching network in fact, thus hindering the all-optical transparent network evolution.

The main impetus of this research, therefore, is to propose a new router architecture based on the pulse position modulation header processing (PPM-HP) scheme that improves processing time and reduces the complexity for an all-optical core router. The

PPM-HP scheme significantly downsizes the look-up routing table and offers robust packet routing regardless of the packet header length and network dimension. In this scheme, an  $N$ -bit packet header address and a look-up routing table are represented in *pulse position modulation* (PPM) format forming a PPM-address and a pulse position routing table (PPRT), respectively. In a PPM-address (i.e. a PPM frame) with length of  $2^N$  slots, a single short duration pulse is located at a specific slot with its position corresponding to the decimal metric of the  $N$ -bit packet header address. In a newly constructed  $M$ -entry PPRT, each entry is a PPM frame comprising a number ( $\leq 2^N$ ) of optical pulses. The locations of the pulses in a PPRT entry  $m$  ( $1 \leq m \leq M$ , where  $M$  is the total number of router outputs) correspond to the decimal values of specific address patterns. This is to ensure that if a packet header address matches with one of the patterns, the router will switch this packet to the specific router's output port  $\#m$ . Correlation between a PPM address and an entry  $m$  of the PPRT can be carried out using only a single bit-wise AND operation in order to check if the packet will be switched to output port  $\#m$  of the router or not. As a result of downsizing the routing table and employing a single bit-wise correlation, the PPM-HP scheme offers an improved processing time for header recognition and minimises SOA-based AND gate gain recovery time. In this thesis, the complete router architecture based on PPM-HP will be presented and all of its key modules will be characterised and investigated.

The second motivation of the research is to improve the ultrafast SOA-based Mach-Zehnder (MZ) optical switches used in the optical header recognition, processing and switching units within the proposed router. New controlling schemes are introduced

including dual control-pulse and unequal control-pulse for terahertz optical asymmetric demultiplexer (TOAD) and symmetric Mach-Zehnder (SMZ) switches, respectively. As a result, these switches offer improved narrow and symmetrical switching window profiles, which directly result in reduced residual crosstalk. In addition, a number of new variants of the MZ configuration have been extended from the SMZ architecture such as Tri-arm Mach-Zehnder (TaMZ) and all-optical chained symmetric Mach-Zehnder (CSMZ) switches which provide a high inter-output on/off contrast ratio in switching and reduced complexity in multiple-channel OTDM demultiplexing, respectively.

The evaluations of the research findings are carried out in analytical calculations and numerical simulations based on the well-known commercial Virtual Photonic Inc. simulation software (VPI) [50]. The operation principle of individual modules and a complete router are characterised and analysed. Furthermore, the further work and the vision of the proposed PPM-HP router are also discussed.

## **1.2 Aims and Objectives**

The main aims of this thesis are to propose and analyse a new packet-switching router based on PPM-HP and to improve the ultrafast MZ-based optical switch crosstalk and contrast ratio performances for optical header recognition. The key objectives are outlined as follows:

- Proposing the PPM-HP concept and designing a complete PPM-HP router architecture for single wavelength and WDM packet switching. This task

includes the formation of a novel PPRT and address correlation mechanism with single-bitwise AND operation.

- Proposing and analysing individual modules of the proposed PPM-HP router such as the clock extraction module, the PPM address conversion module, the PPRT, the optical AND gate, the optical switch controller (including all-optical flip-flop and multiple-pulse generation) and the optical switch.
- Improving residual crosstalk of Mach-Zehnder based optical switches (TOAD and SMZ) and developing a novel Tri-arm MZ-based switch (TaMZ) and multiple-channel demultiplexer (CSMZ) to achieve a high switching contrast ratio and reduced complexity in multiple-channel OTDM demultiplexing, respectively.
- Analytically investigating, evaluating and simulating router operation and its performance. In addition, the work in this thesis demonstrates multiple transmission-mode capability (unicast, multicast, and broadcast) of the router's optical layer.
- Investigating multiple-hop routing performance including accumulated optical signal to noise ratio (OSNR) and propagated crosstalk.

### 1.3 Chapter Outline

The thesis is organised into eight chapters as outlined below:

*Chapter 1 - Introduction* - It presents the research fundamentals and states the aims, objectives and original contributions of the research work. Thesis structure and its content are also outlined.

*Chapter 2 - Literature Review of All-Optical Routers and Ultrafast Optical Switches* - It gives an overview of routing in all-optical packet-switching networks including optical header processing and all-optical switches used for ultrafast optical processing. The issues, drawbacks and challenges in current all-optical routing schemes are highlighted and discussed to pave the way for the introduction of a core router based on PPM-HP.

*Chapter 3 - Terahertz Optical Asymmetrical Demultiplexer Switch* - This chapter first presents backgrounds of SOA and its nonlinearity properties. Subsequently, TOAD optical switch is introduced as a fundamental SOA-based optical switch. The chapter highlights the issues in the existing TOAD switches and proposes new dual control-pulse scheme for improving TOAD switching window (SW) profile which result in reduced residual crosstalk in switched signal. The resultant improved bit error rate and power penalty are investigated and compared with that in conventional TOAD switch.

*Chapter 4 - Mach-Zehnder Optical Switches* – It presents SMZ switch and proposes an unequal control-pulse scheme for its SW profile improvement and residual crosstalk

suppression. New variants of MZ switches such as TaMZ and CSMZ switches will be derived from SMZ architecture which offer high contrast ratios in switching and reduced complexity in multiple-channel OTDM demultiplexing, respectively. Chapter 4 also carries out the characterisations of the newly proposed switches and explores their operation stabilities.

*Chapter 5 - Router with a Pulse-Position-Modulation-based Packet Header Processing Unit* - The chapter introduces the concept and mathematical modeling of the proposed packet switching router based on the PPM-HP scheme. It begins with a PPM-HP based single-wavelength router and extends to multi-wavelength router (WDM router). Individual key modules and their functionalities within the router are also outlined.

*Chapter 6 - PPM-HP Router Modules* - Chapter 6 presents the characterisation and the analysis of the modules in the PPM-HP router. It begins with the clock extraction module (CEM), which is essential to provide correct synchronisation between incoming data packets and other modules within the router. Header recognition including PPM-address conversion (PPM-ACM), PPRT and a bank of optical AND gates is next described. The main optical packet switching unit will be explained where its optical switch controller utilising all-optical flip-flop (AOFF) or multiple-pulse generator and an array of SMZ switches are discussed in detail.

*Chapter 7 - Router Simulations and Performance Investigations* - This chapter verifies the operation of single and multiple-wavelength PPM-HP routers through simulations



carried out in VPI software. Modelling and simulation investigations of noise and crosstalk performance in multiple-hop routing based on PPM-HP will be analysed and confirmed by simulation work. The router input/output characterisation, router features and the summarised specifications of the proposed PPH-HP router will conclude the chapter.

*Chapter 8 - Conclusions and Future Work* - A summary of the research work, findings and drawbacks are presented. The chapter continues by proposing new ideas for further developments of a more efficient PPM-HP scheme and discusses the outlook of optical signal processing and optical memory development employing for a packet switching router.

## **1.4 Original Contributions**

This thesis contains a number of key original contributions summarised as follows:

- Proposal and development of a new PPM header processing concept for ultrafast packet-switching networks. The findings include the proposal of novel PPRT and a single-bitwise AND correlation mechanism, discussed in detail in Chapters 5 and 6.
- Proposal and analysis of a number of new all-optical processing modules such as clock extraction module based on two-inline SMZs (Section 6.2), PPM address conversion module (Section 6.3), pulse-position routing table (Sections 5.3 and

6.4) and all-optical flip-flop (Section 6.6) used to construct the proposed PPM-HP router.

- Investigation and evaluation of the characteristics of a complete  $1 \times M$  PPM-HP router including PPM-HP performance (Section 7.3), noise and crosstalk (Section 7.4), input/output power characterisation and router features (Section 7.5). In addition, the thesis elaborates mathematical models for accumulated optical-signal-to-noise ratio and propagation data-control crosstalk in multiple-hop PPM-HP routing scenario (Sections 7.4).
- Proposal and evaluation of novel controlling schemes for TOAD and SMZ switches to improve switching window profiles which directly result in reduced residual crosstalk in all-optical high-speed switching and OTDM demultiplexing. Details of the proposed controlling schemes are discussed in Section 3.3 and 4.1 for TOAD and SMZ, respectively.
- Proposal and study of the performance and operation stabilities of a novel  $1 \times 2$  TaMZ switch with a high on/off inter-output contrast ratio for switching and a novel  $1 \times M$  CSMZ for multiple-channel OTDM demultiplexing (Sections 4.3 and 4.4, respectively).

## **CHAPTER 2**

# **LITERATURE REVIEW OF ALL-OPTICAL ROUTERS AND ULTRAFAST OPTICAL SWITCHES**

### **2.1 Introduction**

There has been a tremendous progress in research to increase the long-haul transmission distance and to exploit the virtual unlimited transmission bandwidth (70 THz [51]) of the optical fibre in today optical fibre communication networks. Nowadays, the transmission distance as long as 1,250,000 km and the achieved capacity up to several Tbit/s via a single optical fibre are feasible [52-56]. These achievements are due to the design and manufacture of the low attenuation ( $< 0.25$  dB/km) optical fibres at S- and L-bands [5, 51, 57], long-haul dispersion management [6, 58-60], inline broadband optical amplifiers [5, 60-63], signal regeneration (reshaping, retiming, re-amplification) [64],

forward error correction (FEC) [65-67], short-width (picoseconds) pulse sources [68-70] and ultrahigh-capacity optical demultiplexing techniques such as OTDM [8, 71] and DWDM [52, 54, 72].

Nevertheless, the growth of e-services and e-applications in internet has impacts not only on the efficient exploitation of the network traffic bandwidth, which is no longer a main issue in today's network design, but also on the geographical network topology developments. Those networks include Metropolitan Area Network (MAN), Wide Area Network (WAN), Core, Metro, Access (FTTH) and indoor networks [3, 20, 22, 57, 73], see Figure 2.1 [51]. Therefore, the increase in demand for routing optical data entirely in the optical domain imposes many challenges such as the ability of the network to efficiently and economically process and switch a huge amount of optical data at every router.

In this chapter, a comprehensive literature review of all-optical router, header recognition and switching are presented. Section 2.2 outlines optical routing using circuit switching, burst switching and packet switching. Section 2.3 overviews the packet switching router and header recognition schemes being utilised for ultrafast routing. Ultrafast optical switches (UF-OSW) employed in signal processing and switching in a packet switching router will be delineated in Section 2.4. Finally, Section 2.5 will conclude this chapter and discuss the proposed PPM-HP-based router and UF-OSW being investigated in this thesis.



**Figure 2.1** Multiple-layer optical networks [51]

## 2.2 All-optical Routing

Photonic networks are the foundation of modern ultrahigh-capacity communication networking systems. In these networks, all-optical routing is the major factor to optically realise data switching due to its significant impact on the overall network performance. Optical routing (switching) techniques are mainly categorized into three types: optical circuit switching (OCS), optical burst switching (OBS) and optical packet switching (OPS) [3, 51, 74]. Table 2.1 summarises the major characteristics of the three different switching technologies based on their scales, utilisations and complexity.

Among these switching technologies, OCS has the coarsest switching granularity owing to fibres and wavelength bands or wavelengths (wavelength routing) being switched in a circuit-switched WDM network. Wavelength routed networks can be realised by utilising commercially available large-scale switching fabrics such as optical cross-connect (OXC) switches [75-79]. Granularity in burst switching is moderate since the IP packets are aggregated to bursts with sizes of several tens of kBytes in OBS networks [80, 81]. In this technology, an optical transport network sets up an end-to-end connection and reserves resources for the duration of the burst only, which is not supported in OCS. In contrast, in a packet switching network, routing is done on a packet-by-packet basis, with a size of hundreds to a few kBytes, thus providing the finest granularity [23, 48, 82].

**Table 2.1** Comparison of major characteristics of OCS, OBS and OPS [51]

Switching technologies	Granularity	Utilisation	Complexity
Circuit switching	coarse	poor	low
Burst switching	moderate	moderate	moderate
Packet switching	fine	high	high, not mature

In comparison to a fixed-connection OCS, both OBS and OPS are capable of supporting dynamic traffic and therefore, improve the utilisation of the network resources. The advantages of OBS over the conventional circuit switching are: (i) no need for assignment of a dedicated wavelength or waveband for each end-to-end connection

since the connection is set up during the burst period only and (ii) ability to achieve high bandwidth utilisation with a lower average processing and synchronisation overhead than pure packet switching by avoiding a lengthy packet-by-packet operation. OPS is most suitable for dynamic and reconfigurable routing as different packets can be routed in different paths to reach a destination, thus ensuring reduced network traffic latency and congestion. Routing-path decisions are managed by a network management mechanism, which constantly updates the routing information at every network router to deal with the current network blocking status. In the next section, a more in-depth discussion of OPS will be presented.

The complexity of OCS is relatively low while for OBS and OPS, faster switching time and improved processing capabilities are much in demand which, therefore, requires additional control/management, buffering and signal processing functions. However, since burst and packet switching provide high network scalability and upgradeable capability for network functions, the associated cost of expanding OBS and OPS networks will be more economical in comparison to OCS.

Note that each of these optical switching technologies has its own vital application domain; therefore, it would be highly beneficial to integrate these technologies as much as possible instead of being solely used as a replacement for one another. In Section 2.3 an up-to-date literature review will be further presented to identify the main issues in today's OPS network.

## **2.3 All-optical Packet Switching Core Router and Header Recognition Schemes**

### **2.3.1 All-optical packet switching core-router and key components**

A photonic packet switching core-network consists of optical fibre systems with optical core routers (core nodes), edge routers (edge nodes) which are identified by their unique addresses and the fibre links in between, see Figure 2.2. In a core network, packets are routed from a source edge router (ingress router) to a target edge router (egress router) via a defined shortest path through a number of core routers. The shortest-path details are stored in a look-up routing table at each intermediate router. At an ingress router, data packets from client networks with the same (egress router) destination are temporally multiplexed into optical high-speed packets at high bit rates [22, 83, 84]. Upon entering the core network, synchronisation and address (label) details are added to the data packet prior to transmission to the core routers.

An all-optical packet switching core router typically comprises of a number of key and optional modules such as packet synchronisation, header extraction, header recognition, a look-up routing table (or seed pattern generator), a switching unit and (optional) signal processing (for reconfiguration of the router look-up table, buffering, 2R or 3R and equalization), see Figure 2.3. A transmitted data packet basically comprises of the clock signal, header (destination address) and packet payload as shown in Figure 2.4.



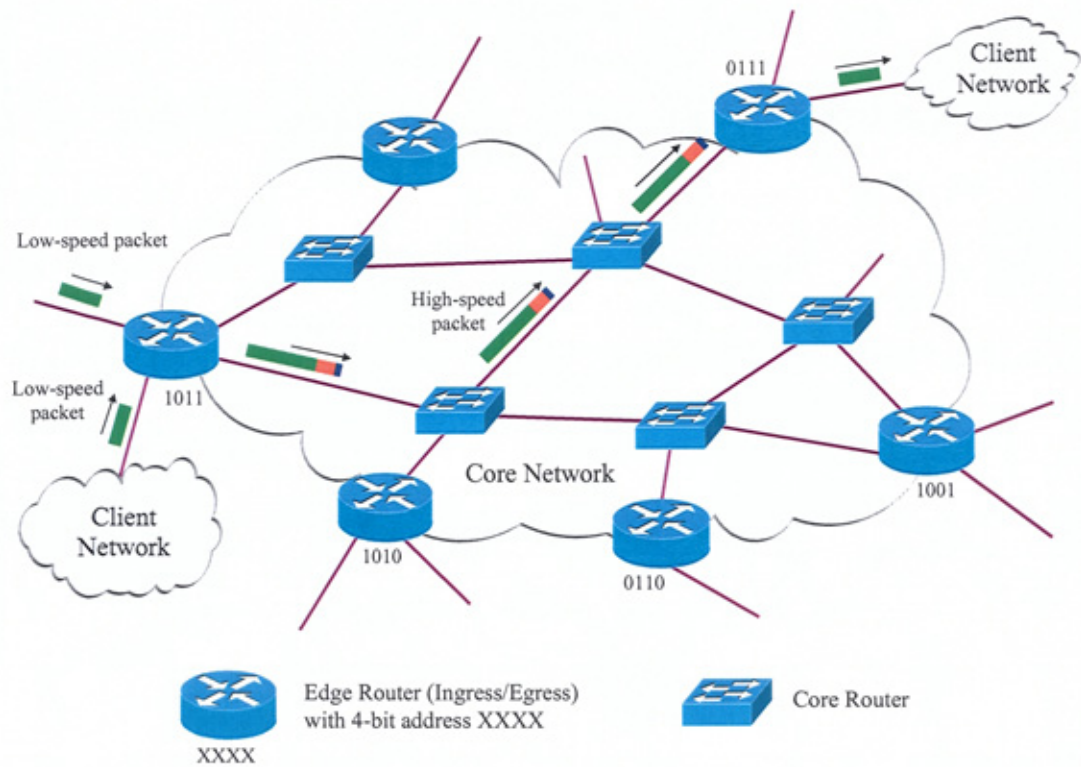


Figure 2.2 Optical core network with edge and core routers

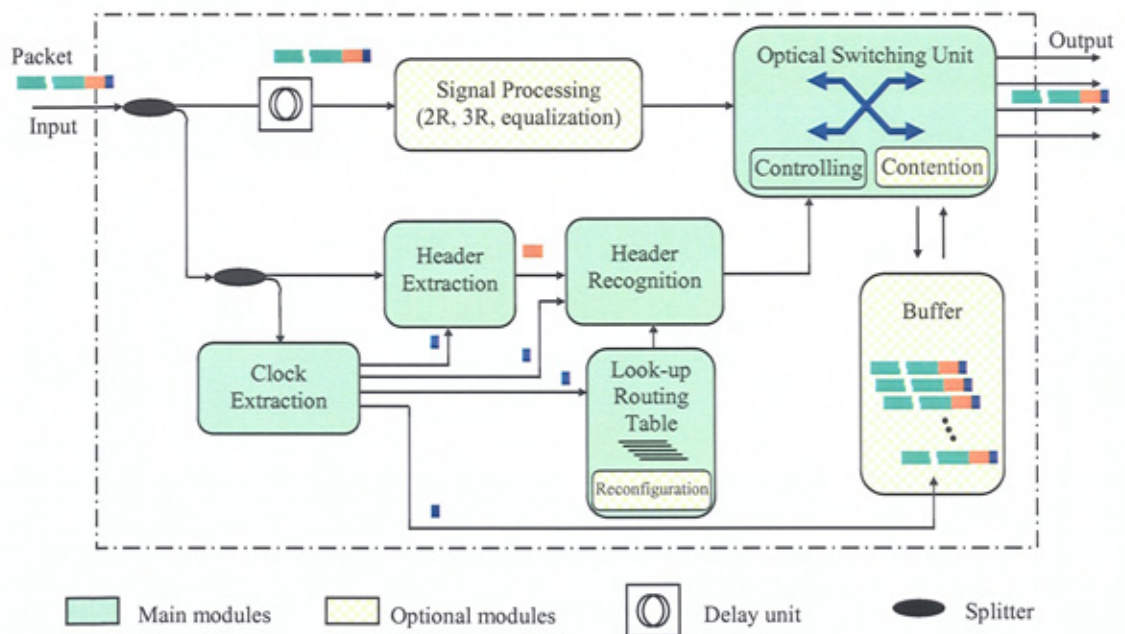
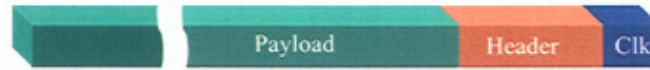


Figure 2.3 A typical  $1 \times M$  optical packet switching router architecture



**Figure 2.4** A typical optical packet format: clock, header and payload

In Figure 2.3, packets arrive and are passed through a  $1 \times 2$  splitter. The main portion (power) of the packet is delayed in the delay unit while it waits for the router to make its routing decision before being switched. The other portion is used for synchronisation, header extraction and signal processing modules. The extracted clock signal is used for synchronisation. The header extraction module extracts and converts packet address bits into a format suitable for the header recognition module. The header recognition module will carry out packet address correlation based on the routing information in both the packet header address and routing table, the matching output of which is used as the control signal for the main optical switching unit, thus ensuring that the incoming packet is switched to the right output port of the router. Inclusion of optional modules such as a reconfigured look-up routing table, buffering and signal processing will provide additional functions that improve the routers non-blocking characteristic (contention solution) and boost optical signal quality [16, 33, 85-92].

There are two methods of clock extraction for optical system synchronisation based on the incoming packet clock signal: (i) using an internal clock source (a laser source generating an optical-pulse stream) that needs to be in-phase with the incoming packet [36, 37, 93-95] and (ii) self-extracting the clock pulse from the incoming packet [17, 22, 96, 97]. In the first approach, a phase-locked loop is employed to detect and compensate for the delay difference between the internal clock and received packets. However, the

use of this method is limited because of a long acquisition and locking time and a costly internal laser source (with no jitter) [95]. Clock self-extraction offers a reduced hardware complexity and avoids the locking latency by extracting and directly reusing the clock signal (pulse) in the optical domain [21, 97]. A number of self-extraction clock recovery schemes based on the ultrafast optical switches incorporated with an all-optical feedback loops have been proposed [17, 98]. Though these schemes require a minimum number of ultrafast optical switches, a carefully constructed feedback-loop is a strict requirement to ensure operation stability and a complete suppression of the residual signals following the desired extracted clock signal. Moreover, the temporal delay associated with the fibre or optical waveguide feedback-loop will limit the response and operation speeds of feedback-based clock recovery. All-optical clock recovery with two inline optical switches is proposed in this thesis where a feedback loop is no longer required (Section 6.2) which reduces the clock extraction complexity.

Routing decision is obtained by determining the destination address for the next routing hop. In general, there are two main mechanisms for obtaining a routing decision in ultrafast all-optical networks based on: (i) predefining a routing path by embedding the controlling bits in the packet header to directly switch individual routers' switches on or off, thus all switches' states are required to be prior-known [17, 21] and (ii) embedding only the destination address in the packet header, thus enabling the correlations of the packet header with the entire routing look-up table entries stored in each intermediate router [7, 12, 13, 22, 99]. The latter scheme is preferable because: (i) it shortens the packet-header length and (ii) it relieves the bulky network traffic management task. This

is because the task of updating the routing-table is performed in a distributed router level, i.e. each router reconfigures its own look-up routing table according to its location in the network and the network traffic status, instead of being done at each edge router (centralised) which hence, requires the updating of full-lists of routing paths at every other edge router. A further discussion on all-optical header recognition schemes will be developed in the Section 2.3.2.

The optical switching unit could be implemented based on the existing enabling switching technologies such as opto-mechanical [78, 100, 101], opto-thermo [102], optoelectronic [103, 104], liquid crystal [105, 106], bubble [107, 108] and ultrafast all-optical switches (UF-OSW) based on the SOA [28, 109-112]. Among these approaches, UF-OSW is preferable in ultrahigh-speed switching applications as it has three main desirable characteristics: (i) directly controllable capability using low-energy optical pulse(s) [41, 113], (ii) fast switching response as short as a narrow optical pulse-width (in picoseconds) [27, 31, 32, 114] and (iii) switching duration flexibly, which varies from a few picoseconds to nanoseconds [9, 11, 36, 115], whereas other switches have responses of the orders of in milliseconds or microseconds [108]. Further details of ultrafast all-optical switches will be highlighted in Section 2.4 and studied in Chapters 3 and 4.

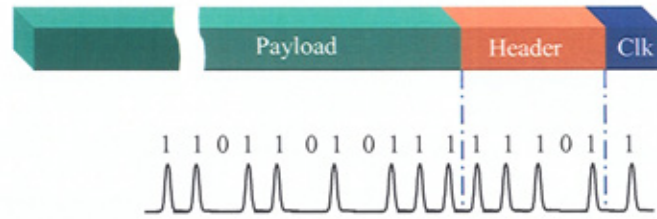
### **2.3.2 Packet header and header recognition**

In a packet switching network, a packet header address is used to make a routing decision at intermediate routers in a routing path. There are a number of approaches to

optically encode a packet header address such as using a set of on/off bits for directly controlling the on/off states of individual switches at each intermediate router (node) in the routing path [17, 21, 116, 117], multi-wavelength address [118-121], PPM-encoded address [122, 123] and binary encoding address [3, 5, 13, 22, 84]. The on/off-bit addressing method provides the simplest self-routing design but it enlarges the header length proportionally with an increase of hops in a long routing path. In a multi-wavelength encoded address, an individual address bit could be encoded by one of a number of specific wavelengths, thus offering a considerable number of combined addresses (theoretically up to 4 billions [121]). However, there is an extensive requirement of hardware resources which deter the performance and scalability of networks employing this scheme in reality. A PPM-encoded address comprises a bit located at a specific position designed for a unique address pattern. This encoding scheme ultimately offers a direct correlation between packet header address and the proposed pulse-position-routing-table in a PPM-based router [123], which speeds up the header correlation time compared to existing header correlation schemes. However, this technique is susceptible to the optical dispersion and timing jitter in a long optical fibre link and requires a long packet prefix increased with the number of edge routers. Binary encoding, i.e. containing single-wavelength on/off optical pulses, is a conventional addressing method in optical data communications where an  $N$ -bit packet header address could encode up to  $2^N$  destination node addresses. An  $N$ -bit binary-encoded address could be in one of two fundamental line coding schemes such as Non-Return-to-Zero (NRZ) and Return-to-Zero (RZ) [3, 5, 124]. In this thesis, narrow-width optical pulses (the RZ scheme) will be used for data transmission and routing.



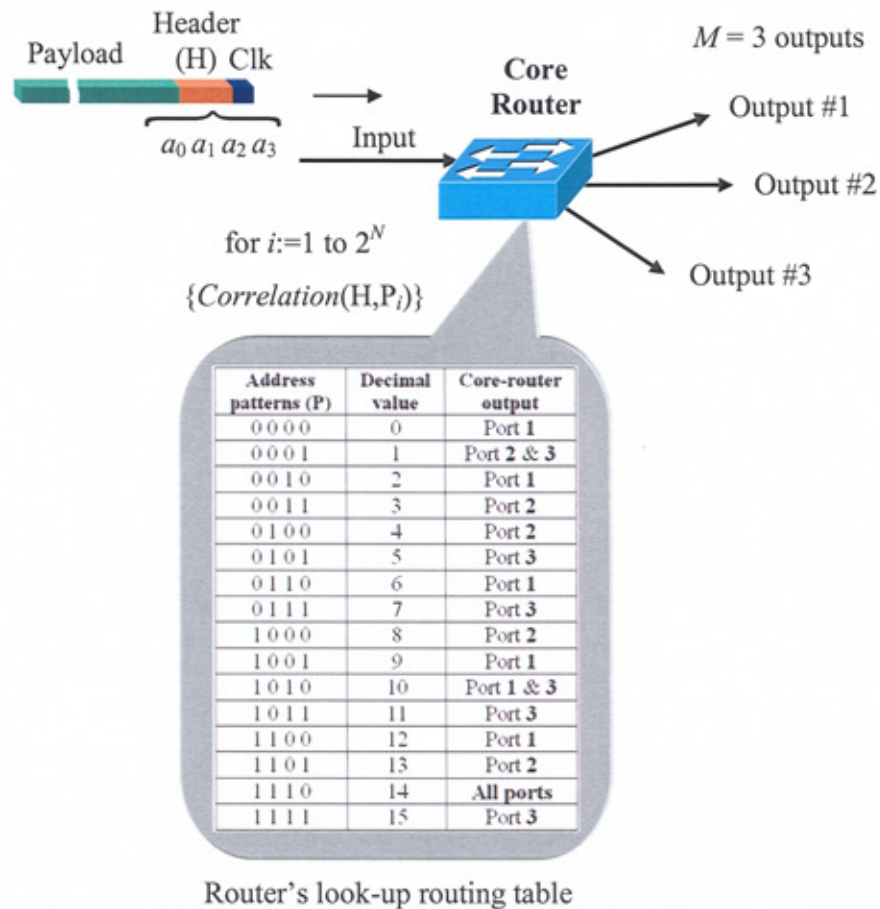
In addition to encoding techniques, header address and clock signal are attached and transmitted with the payload using different mechanisms such as wavelength-multiplexing using sub-carrier modulation (SCM) for all-optical label switching (AOLS) in a multi-protocol label switching (MPLS) network [15, 22, 33, 125], cross-polarisation [126], different bit rates [127], unequal intensities [128, 129] and time-multiplexing [98]. Among the proposed schemes, multiplexing of a clock signal with a binary-encoded header and payload in the time domain having the same intensity, wavelength and polarisation, see Figure 2.5, is a preferred option and adopted in this thesis due to it being relatively low complexity in comparison to other schemes.



**Figure 2.5** Optical packet binary-encoded and time-demultiplexed formation with a clock pulse (1 bit), header ( $N = 5$  bits) and payload

In a core-router, header recognition of a binary-encoded header address is carried out by correlating the header address with the entire address patterns stored in a look-up routing table, see Figure 2.6. The routing table contains all possible address patterns (or an addressing range) and the associated output ports of the router for the packet to be switched to [16, 22, 43, 99]. Typically in a core network, an intermediate router has a limited number of output ports [22, 130]. When there is a matching correlation between

the packet header address and a particular address pattern, a pulse signal is generated to open the corresponding router's output port of which the output port index is given from routing table. Therefore, the router switches the input packet to that intended output port.



**Figure 2.6** Router look-up routing table (16 possible patterns **P** for  $N = 4$ ) at the core-router and sequential correlations

A range of address correlation schemes have been proposed for all-optical header recognition including optical Boolean logic gates [38, 131-139], an optical correlator

[16, 43], two-pulse correlation [122, 140], time-stretch pre-processing [141], time-axis header processing [142] and time-to-wavelength conversion [46]. The logic gate is based on peculiar nonlinearity phenomena of the SOA such as cross gain modulation (XGM), cross phase modulation (XPM) and four-wave mixing (FWM) in combination with an optical interferometer [11, 25, 32]. In the proposed ultrafast nonlinear 2-input XOR, AND and OR gates, a pair of pump (high power) and probe (low power) optical signals are simultaneously injected into the interferometer as two inputs and the Boolean logic output is observed from the output probe signal at the interferometer output. The interaction between a pump signal and SOA instigates nonlinear changes in both SOA gain and phase, thus simultaneously impacting the gain and phase characteristics of the probe signal (with low power level inducing negligible effect on the SOA nonlinear changes) [32, 114]. Since the depth of the SOA gain saturation level depends on the power of the pump signal, the SOA gain recovery time also depends on the pump signal. As a result, the gate response and a repetition speed of logic gates based on SOAs are constrained by the SOA gain recovery characteristics and input optical pulse power. Optical logic gates offer an ultrafast response (a few picoseconds) and high operating bit rate of up to 100 Gbit/s [7, 136]. An optical correlator is implemented using either a mirror-reflection array or a controlled fibre Bragg grating (FBG) in combination with an intensity threshold detector to detect the matching signal power during cross-correlation between the packet address and a RT entry. Although this scheme could operate at a high speed (40 Gbit/s), it suffers from a number of drawbacks such as implementation complexity and low-speed electrical threshold detecting [16]. Two-pulse correlation is employed to recognise a specific long header pattern using a single TOAD. An aspect of



the concept is that the address information is encoded by the difference in time between the leading edges of two header pulses. The resultant correlation output is detected by the timing alignments among header edges and an assisted control pulse [122]. This concept is suitable for long-header address recognition, however, it is limited by a specific edge-timing header encoding scheme which hinders potential applications in optical networks based on conventional binary-encoded packet addresses. The time-stretch pre-processing scheme can relieve the speed requirement of logic gates or correlators by stretching the packet header in the time domain, i.e. slowing down the packet header rate, for performing low speed header processing in electrical domain. The all-optical time-axis header processing approach exploits the binary pattern in the header address to generate a pulse whose location matches with the decimal metric of the header address. Upon matching pulse generation, a circuit switching path in the switching matrix is set up to route an input packet. The proposed scheme is conceptually impressive, but it is not feasible for a long address pattern (i.e. requiring an additional number of switching stages [142]) due to the increase of accumulated noise and crosstalk in the routed packet from serial-connected switching stages. Recently, an asynchronous all-optical header processing scheme, based on time-to-wavelength conversion, has been proposed which offers high scalability using only four optical switches for recognizing a large number of specific headers [122]. In this scheme, the header processor produces a pulse whose wavelength is uniquely determined by the input packet header. Nevertheless this scheme requires a PPM-encoded header address, thus increasing the packet overhead with the number of header patterns.

In summary, the key technological issues in all-optical header recognition are highlighted as below:

- 1) Speed and robustness of header recognition.
- 2) Size of look-up routing table.
- 3) Complexity and scalability properties when upgrading and expanding core network (i.e. adding/dropping core router).

In Chapter 5, the concept and architecture of a packet switching router, based on a novel PPM-based header recognition of a binary-encoded header, is introduced as one of the potential solutions for the improvement of the issues highlighted. Section 2.4 will next overview different ultrafast all-optical switches as building blocks to implement the optical processing and routing in an OPS network.

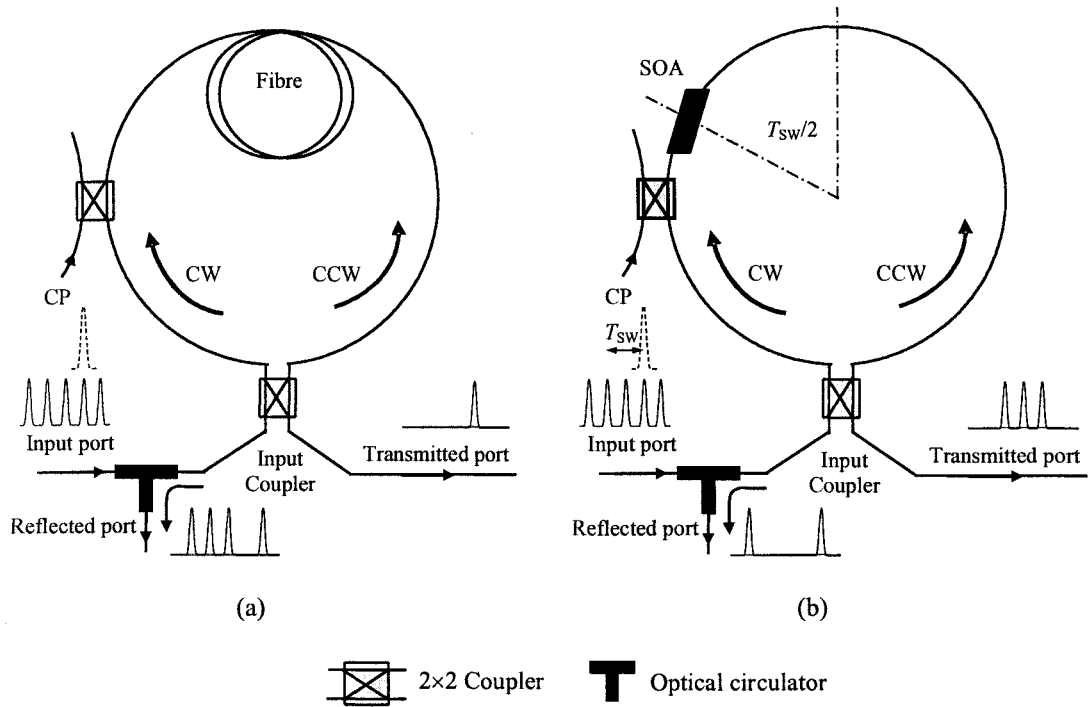
## **2.4 Ultrafast All-optical Switches**

Technological changes are taking place in both long-haul and access optical communications networks, which in turn open up opportunities for research in new areas such as complex network and traffic theory, multiplexing, high-speed devices for all-optical switching and signal processing, etc. Photonic networks are designed to offer not only increased capacity with a low operation cost, but also greater functionality. In recent years there have been great efforts in research activity for the development of ultrafast all-optical switches (offering fast responses, narrow switching windows and lower required control power) as the building blocks for optical functions in photonic

networks such as: all-optical synchronisation [36, 94], header recognition [143-145], optical switching [146, 147], wavelength conversion [35, 148], 3R [33, 89], optical memory [149, 150], multiplexing/demultiplexing [8, 151] which provides low bit error rates in all-optical end-to-end transmission [42, 152]. Therefore, a thorough understanding of these all-optical switches and their applications in optical signal processing functions is a crucial factor to realise a complete all-optical router successfully.

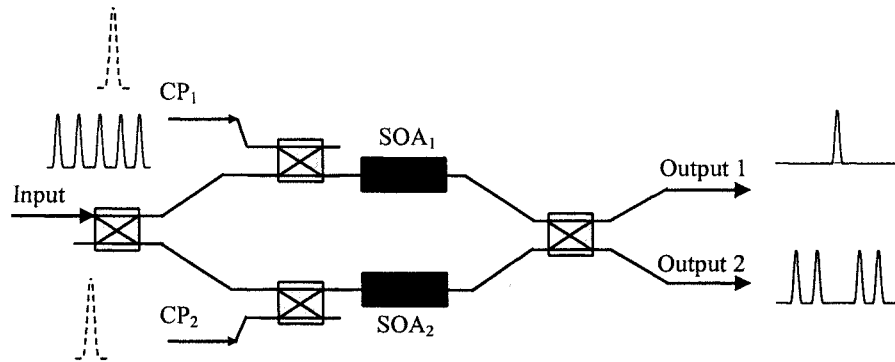
A number of well-known all-optical switches, such as the nonlinear optical loop mirror (NOLM) [153, 154], the terahertz optical asymmetric demultiplexer (TOAD) [28, 109, 155], symmetric Mach-Zehnder interferometers (SMZ) [55, 110], and the ultrafast nonlinear interferometer (UNI) [111], have been proposed and widely employed in photonic networks. The NOLM consists of a long loop of nonlinear fibre coupled by a  $2 \times 2$  coupler, see Figure 2.7(a). Without the control pulse, the input signal entering the NOLM input port is split into clockwise (CW) and counter clockwise (CCW) components propagating within the loop, recombining again at the  $2 \times 2$  coupler and emerging from the reflected input port. In the switching mode, a high-powered control pulse (at a different wavelength) is pumped, before the arrival of the CCW component, into the loop via a coupler, thus introducing a nonlinear effect by changing the refractive index of the fibre loop. This results in a phase difference between CW and CCW components. Consequently the recombined signal will emerge from the transmitted output port. Though the NOLM temporal switching window (SW) width is narrow (a few picoseconds), it requires high power control pulses and a long length of fibre

(typically having a weak nonlinear property) to provide a sufficiently nonlinear phase shift change for high-gain switching. The TOAD switch, shown in Figure 2.7(b), is composed of a short interferometer optical fibre loop with a semiconductor optical amplifier (SOA) positioned in a fixed location offset from the loop centre (equivalent time delay of  $T_{sw}/2$ ). The SOA is used to achieve the nonlinear effect, thus inducing the phase shift between CW and CCW components instead of using long fibre as the NOLM scheme. Nevertheless, its switching performance in ultrahigh-speed applications ( $>100$  Gbit/s) is limited because of its fixed and asymmetric SW profile, owing to the fixed SOA location and the counter-propagation effect between the input data and control signals within the SOA [9, 74, 156], respectively.



**Figure 2.7** Ultrafast optical switches: (a) NOLM and (b) TOAD

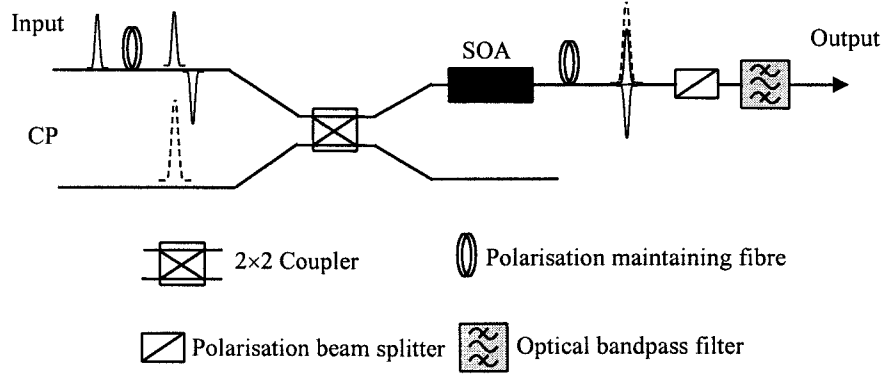
The SMZ switch overcomes these limitations by using an optical interferometer comprising of two identical arms each with an identical SOA, see Figure 2.8. This configuration will ensure that the induced nonlinearity effect on the propagating input data signals are controlled as fast as control signals are injected into both SMZ arms. Since both input data and control signals propagate in the same direction within SOAs, the response of the SMZ switch is as fast as the pulse width, and SMZ has a symmetrical narrow SW width (a few picoseconds) [25, 37, 157, 158]. In addition, SMZ-type switches offer a superior integration capability whilst operating with a lower control power energy ( $<1$  pJ) [9, 25, 41] in comparison to the TOAD.



**Figure 2.8** Optical SMZ switch

In the UNI switch, depicted in Figure 2.9, the SW is achieved by the phase difference between the two orthogonal polarisation components of the input data signal provided by the fast nonlinearity of the SOA through its interaction with the second control pulse whenever it is present [7, 147]. However, due to the fibre birefringence and polarisation control, the UNI offers a poorer integration capability in comparison to the SMZ switch. Therefore, among these switches, the SMZ is the most promising switching architecture

suitable for ultrafast switching and signal processing. In this thesis, the SMZ is used as the building block for implementation of the PPM-HP based router.



**Figure 2.9** Optical UNI switch

Further details of the TOAD, SMZ switches, MZ variants and their applications for PPM-HP router will be presented in Chapters 3, 4 and 6, respectively.

## 2.5 Summary

In this chapter, an overview of all-optical switching, header recognition and ultrafast all-optical switching were presented. The chapter began with an introduction to optical switching technologies where packet switching was considered as one of the most appropriate approaches for dynamic and reconfigurable packet routing in a packet switching core network. In such a network, an all-optical core router and its main components were described. Packet header recognition is underlined as one of the most essential modules for attaining high routing performance in terms of processing latency and complexity. A number of enabling header recognition techniques were discussed

and compared. The chapter also highlighted the key issues with all-optical header recognition such as look-up routing table size, network expansion scalability and processing robustness. Finally, an overview of ultrafast optical switches employing in all-optical signal processing and switching was provided.

In Figure 2.10, a research road map is presented summarising the research areas and original contributions of this thesis.

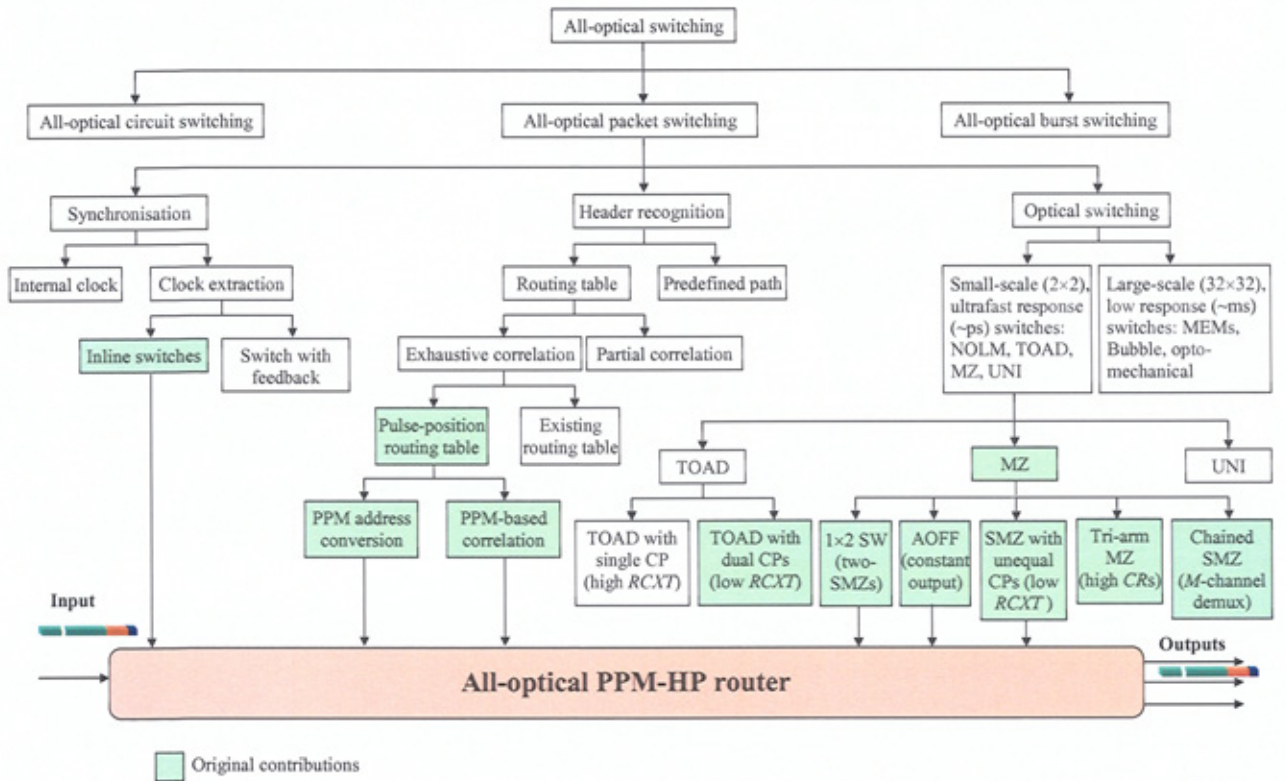


Figure 2.10 Research road map

In the next Chapters 3 and 4, the studies of ultrafast optical switches will be carried out to characterise and improve their crosstalk and contrast ratio performance for the switching and processing applications in OPS.

## **CHAPTER 3**

# **TERAHERTZ OPTICAL ASYMMETRICAL DEMULTIPLEXER SWITCH**

### **3.1 Introduction**

In recent years, research activities in the development of ultrafast all-optical switches as the building blocks for all-optical switching and routing applications have been intensified. Among all-optical switches, ultrafast all-optical switches based on SOAs are the most promising candidates for the realisation of all-optical switching and processing applications through the exploitation of their fast-appearing and strong nonlinearity characteristics [26, 28, 29, 31, 32, 114, 159]. There are three main ultrafast optical switches including TOAD, SMZ and UNI employing SOA nonlinearity in optical constructive/destructive interferometers, which offer ultrafast responses, low switching energy and compact size [9, 11, 25]. In this thesis, the SMZ switch will be studied throughout for use as the building block for the proposed packet switching router.



In this chapter, the background to the SOA is presented and explained. The TOAD switch is introduced as the fundamental optical switch based on the SOA and optical interferometer. Mathematical models for the SOA and TOAD have been well developed in previous literature; therefore they are briefly reviewed in this chapter. The new dual control-pulse (CP) scheme for the TOAD switch will be proposed in order to achieve a better symmetric switching window profile in comparison to that in existing single-CP TOAD configurations. The performance improvements, including reduced residual crosstalk (*RCXT*), improved bit-error-rate (BER) and reduced received power penalties in high-speed switching and demultiplexing, will also be investigated.

### 3.2 Semiconductor Optical Amplifier

The optical amplifier in modern photonic communications is not limited solely to use as an optical signal amplifier but also is an essential component in the ultrahigh-speed switching and processing of optical data in the optical domain [3, 5, 32]. Optical amplifiers are categorised into two classes: optical fibre amplifiers such as the *erbium-doped fibre amplifier* (EDFA) [5, 62, 63], and semiconductor optical amplifiers (SOA). The essential differences between these two classes are (i) the speed of transiently saturating (i.e. gain reducing) and recovering amplifier gain and (ii) the amplifier non-linearity characteristics [5, 25, 32].

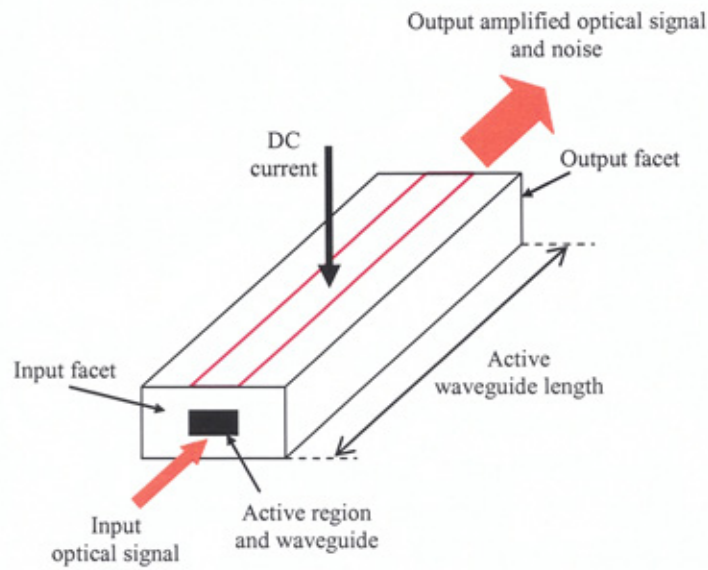
In optical signal amplification, a crucial factor for assuring the invariant signal quality is the amplification gain flatness. Amplification of an optical signal will consume carriers, thereby transiently saturating the amplifier gain. Therefore, to maintain approximately

the same temporal gain for all data bits, i.e. reducing the signal distortion or in other word minimising the patterning effect, the change in magnitude of the gain saturation must be sufficiently small over adjacent bits. This condition can be fulfilled when either the gain recovery time is shorter or much longer than one bit duration [32]. With a gain recovery time in the region of milliseconds for an EDFA in comparison to a few hundreds of picoseconds in a SOA, so far, the EDFA is the preferred choice for inline optical signal amplification in multi-Gbit/s optical communication systems, in which EDFA effectively averages the power of long bit sequences to reduce the patterning effect and dynamic wavelength changes [5]. In addition, the EDFA offers a wide optical amplification bandwidth (40 nm), simplicity, low coupling loss, high gain (with high output saturation power), low polarisation insensitivity and low noise figure ( $NF < 4.5$  dB) in comparison to SOA [5, 62, 63, 160].

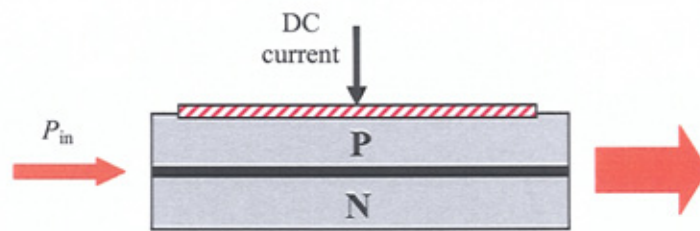
On the other hand, the SOA offers better performance in optical signal switching and processing applications due to its fast gain saturation and strong nonlinearity-response (of the order of sub-picosecond) to the input optical signal [25]. In addition, the SOA has a number of advantages in its design for all-optical systems in comparison to the EDFA such as its compact size (integration capability), low optical and electrical power consumption and high speed. In the light of this, the SOA is widely used in high-speed all-optical switching and processing applications. It is therefore necessary to understand and utilise the SOA in an appropriate manner. The next sections outline the SOA principle and its application in switching.

### 3.2.1 SOA principle

The SOA is basically a semiconductor laser composed of an optical waveguide between a P-N junction with anti-reflection coated facets, which amplifies an injected light signal by means of stimulated emission, see Figure 3.1(a) and (b).



(a)

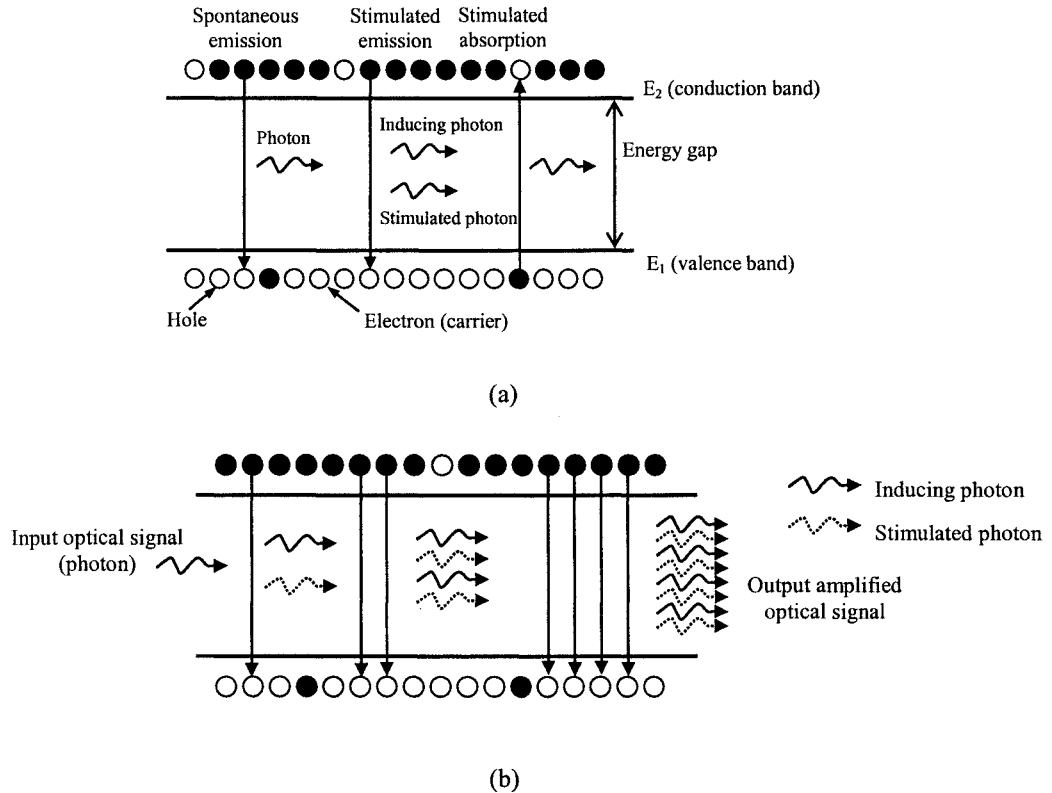


(b)

**Figure 3.1** (a) Schematic diagram of a SOA and (b) optical waveguide and P-N junction in SOA

When a SOA is DC biased, the conduction and valence (energy) bands containing the electrons (carriers) and holes, respectively, are formed, see Figure 3.2(a). When the

energy bands are formed three physical processes [32, 161] take place within the SOA including (i) spontaneous emission, (ii) stimulated absorption and (iii) stimulated emission.



**Figure 3.2** (a) Spontaneous emission, stimulated emission and stimulated absorption processes in SOA and (b) SOA amplification

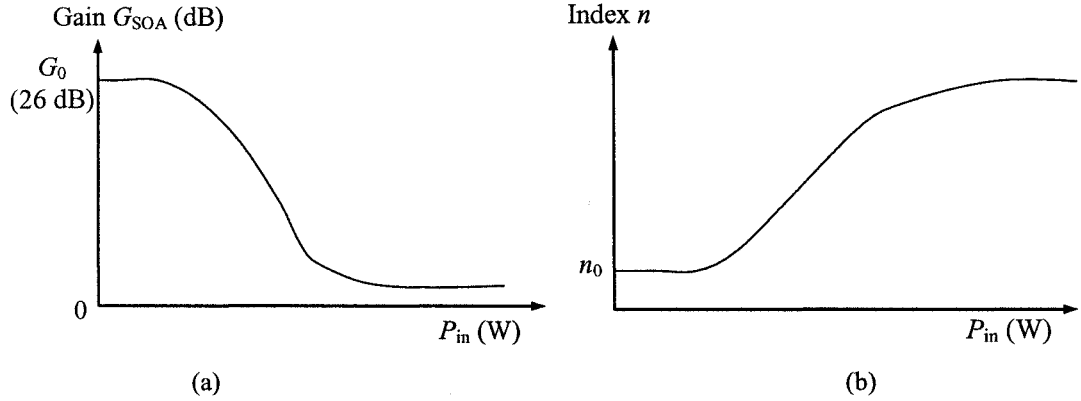
Spontaneous emission is the process in which the excited electron having its energy in the conduction band is dropped to the valence band, thus either releasing a photon or generating heat due to the energy difference between the two bands. The generated photon will be radiated with a random phase and direction, thereby being considered as spontaneous noise of the SOA. The probability of spontaneous emission is increased

with high electron density in conduction band. On the other hand, in stimulated absorption an electron with its energy in the valence band absorbs the energy of an incident photon hence obtaining a higher energy level and moving to the conduction band. The occurrence of stimulated absorption is more frequent when there are many incident photons and high electron density in the valence band. Without a DC biased current/voltage, the electron density in the valence band is much higher than that in the conduction band, thus impeding the SOA amplification, i.e. less photons emerge at the SOA output. The stimulated emission process occurs when an incident photon hits an excited electron with its energy in the conduction band releasing a stimulated photon with the same phase, frequency and direction to that of the incident photon (i.e. amplification). The energy of the electron, therefore, drops to the valence band.

When an optical beam is injected into the SOA from the input facet, see Figure 3.2(b), the input photons interact with the excited electrons in the conduction bands to release extra identical photons along the longitudinal waveguide, thus amplifying the input optical signal. As a result of the excited electron depletion, there is a reduction in the density of excited electrons in the conduction band (i.e. the carrier density) resulting in two consequences:

- (ii) A reduction in SOA gain  $G_{\text{SOA}}$ . This reduction is due to the amplification gain being proportional to the carrier population in the active region; however, carriers are consumed during the amplification, see Figure 3.3(a)

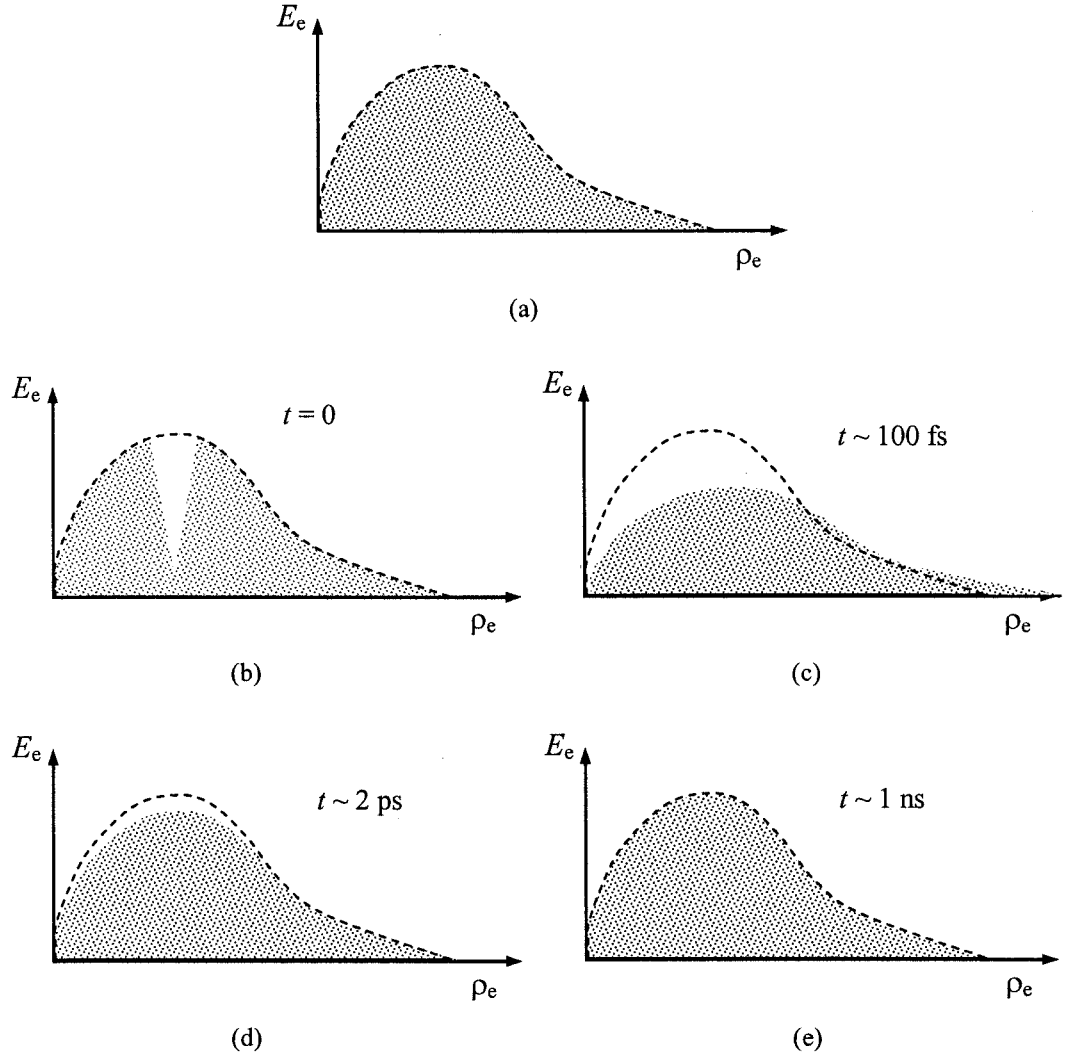
- (iii) An increase in the active waveguide refractive index  $n$  with the increase of the input amplified signal (i.e. intensity dependence), see Figure 3.3(b), due to the nonlinear  $n$  being dependent on the carrier density [26, 28]



**Figure 3.3** (a) Gain saturation against input optical power and (b) refractive index of the waveguide against input optical power

Recovery following depletion is quantitatively described in the following processes. Figure 3.4 depicts the evolution of carrier distribution (electron density  $\rho_e$  against the electron energy  $E_e$ ). Originally, the carrier distribution is in equilibrium with a Fermi-Dirac distribution function, see Figure 3.4(a). The injection of a short optical pulse will initiate the stimulated emission, inducing amplification and hence carrier density depletion, see Figure 3.4(b) at the time  $t = 0$ . From this point onwards, the SOA state, as far as gain and index are concerned, can be characterised by the total carrier density. The carrier non-equilibrium is governed mainly by the spectral hole burning effect (or, in other words, by a localised reduction in the number of carriers at the transition

energies) [162, 163] and by carrier heating (i.e. a transient heating of the electron and hole temperatures) [162-165].



**Figure 3.4** (a) Equilibrium carrier density distribution (Fermi-Dirac), (b) the stimulated emission induced by a short optical pulse (at  $t = 0$ ), (c) the distribution recovers to equilibrium by carrier-carrier scattering, (d) establishing a Fermi-Dirac distribution function and (e) carrier temperature relaxation and carrier injection [32]

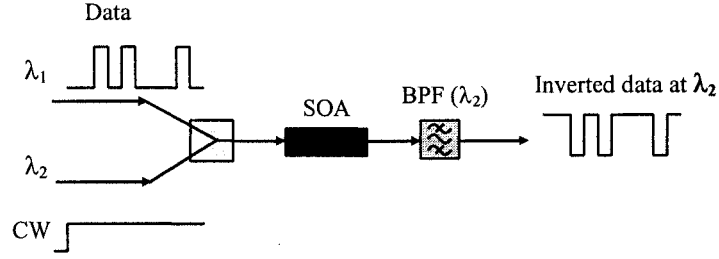
The distribution recovers to equilibrium by carrier-carrier scattering, see Figure 3.4(c). On a 100-fs time scale, instantaneous processes such as two-photon absorption [166, 167] and the optical Kerr effects [168, 169] influence on the SOA response. Within a few picoseconds, a quasi-equilibrium (Fermi-Dirac) distribution is established (see Figure 3.4(d)) due to the carrier temperature relaxation process. Finally, the carrier injection process recovers the carrier distribution to the equilibrium state, as illustrated in Figure 3.4(e).

The SOA gain dynamics are therefore determined by the carrier recombination lifetime. This implies that the SOA nonlinearity features will react relatively quickly to the changes in the input signal power. There are three main resultant nonlinear effects [25, 32] being exploited for all-optical switching and processing: cross-gain modulation (XGM) [146, 170], cross-phase modulation (XPM) [146, 171] and four-wave mixing (FWM) [38, 172, 173].

Figure 3.5 shows the cross-gain modulation of a data signal at wavelength  $\lambda_1$  on a CW probe signal at  $\lambda_2$ , which are simultaneously injected to the SOA. The data signal saturates the SOA gain, thus imprinting its inverted pulse pattern on the probe signal. The XGM configuration is mainly employed in wavelength converters due to its simplicity, stability and fast response [174, 175]. However, XGM-based wavelength converters suffer from limited transmission links on optical fibres with anomalous dispersion. This effect is due to the induced red-shifted and blue-shifted chirps [176],

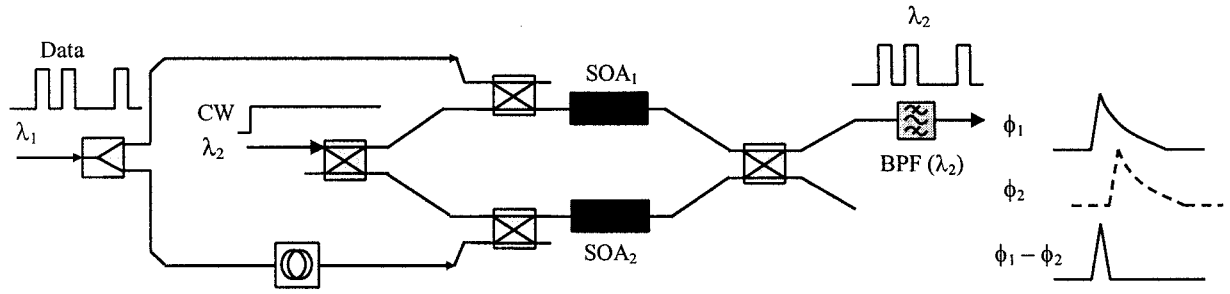


corresponding to the accompanied phase modulation, incurred together with XGM, on the leading and trailing edges of the inverted pulses, thereby resulting in pulse width broadening [32].



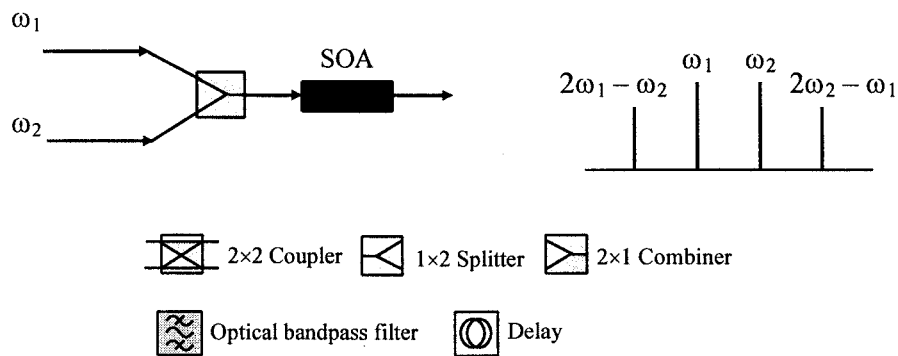
**Figure 3.5** Cross gain modulation (XGM)

The use of SOAs in a Mach-Zehnder interferometer (MZI) overcomes the above limitation in wavelength conversion by exploiting the cross-phase modulation effect. Figure 3.6 depicts a MZI composed of two SOAs located in identical arms including the input/output ports. The data signal at  $\lambda_1$  modulates the phase of the CW signal at  $\lambda_2$  propagating in the upper arm, thus changing the constructive characteristic of the MZI output with respect to the CW signal and hence, switching the  $\lambda_2$  signal out from the interferometer. The duration of the switched pulse is determined by the delay time  $T_{sw}$  of the data signal being injected to the lower arm to compensate for the cross phase modulation, thus restoring the MZI destructive characteristic at the output port. The advantages of XPM used in a MZI are its low optical power requirement and ultrafast switching. However, the main drawback of XPM is the low achieved extinction ratio due to the patterning effect (i.e. different pattern consisting of different 0s and 1s bits) incurred at high bit rates. More details on XPM and the MZI are discussed in later sections in this and the next chapter.



**Figure 3.6** Cross phase modulation (XPM)

Four-wave mixing is a non-linear process which leads to the generation of a number of extra frequencies from the interaction between light at two or three incident frequencies, see Figure 3.7. For the simplicity of representing the modulated signals,  $\omega$  is used instead of  $\lambda$ . FWM has applications in the development of wavelength conversion [177, 178] and all-optical logic gates [38, 179, 180] employing in all-optical routing systems. However, FWM dependency on the relatively low conversion efficiency limits its operation because it requires a relatively small dynamic frequency range of input signal and generates low output power [39, 177].



**Figure 3.7** Four-wave mixing (FWM) and the output frequency spectrum

### 3.2.2 Rate equation

The rate equation used to explain the change of carrier density with respect to the input optical power is given by [25, 26, 28, 155]:

$$\frac{\partial N}{\partial t} = \frac{I_e}{qV_{\text{SOA}}} - R_{\text{sp}} - \frac{P\Gamma g_d(t)}{hf_0 A_{\text{SOA}}}, \quad (3.1)$$

where  $I_e$  is the injection DC current,  $q$  is the electron charge,  $V_{\text{SOA}}$  is the SOA active volume,  $R_{\text{sp}}$  is the recombination rate,  $hf_0$  is the photon energy,  $A_{\text{SOA}}$  is the cross-section area of active region,  $g_d$  is differential gain (i.e. gain per unit length),  $\Gamma$  is SOA confinement factor and  $P$  is the optical power presenting within the SOA.  $g_d$  is given by [1, 28, 161, 181]:

$$g_d(t) = g[N(t) - N_T], \quad (3.2)$$

where  $g$  is gain coefficient,  $N(t)$  is the SOA carrier density (for electrons as well as holes) and  $N_T$  is the carrier density at transparency.

There are two mathematical definitions for  $R_{\text{sp}}$ . A simple one, given by [25, 26, 182, 183]:

$$R_{\text{sp}} = \frac{N}{T_{\text{sp}}}, \quad (3.3)$$

and a more complex definition given by [146, 184-186]:

$$R_{\text{sp}} = A \cdot N + B \cdot N^2 + C \cdot N^3, \quad (3.4)$$

where  $A$  is the surface and defect recombination coefficient ( $\text{s}^{-1}$ ),  $B$  is the radiative recombination coefficient ( $\text{m}^3\text{s}^{-1}$ ),  $C$  is the Auger recombination coefficient ( $\text{m}^6\text{s}^{-1}$ ),  $N$  is carrier density and  $T_{\text{sp}}$  is the spontaneous emission time (carrier lifetime).

In this thesis, (3.3) is used in developing the theoretical SOA model for simplicity, whereas (3.4) is adopted in the numerical simulation model as in the commercial Virtual Photonics Inc. (VPI) simulation software [50].

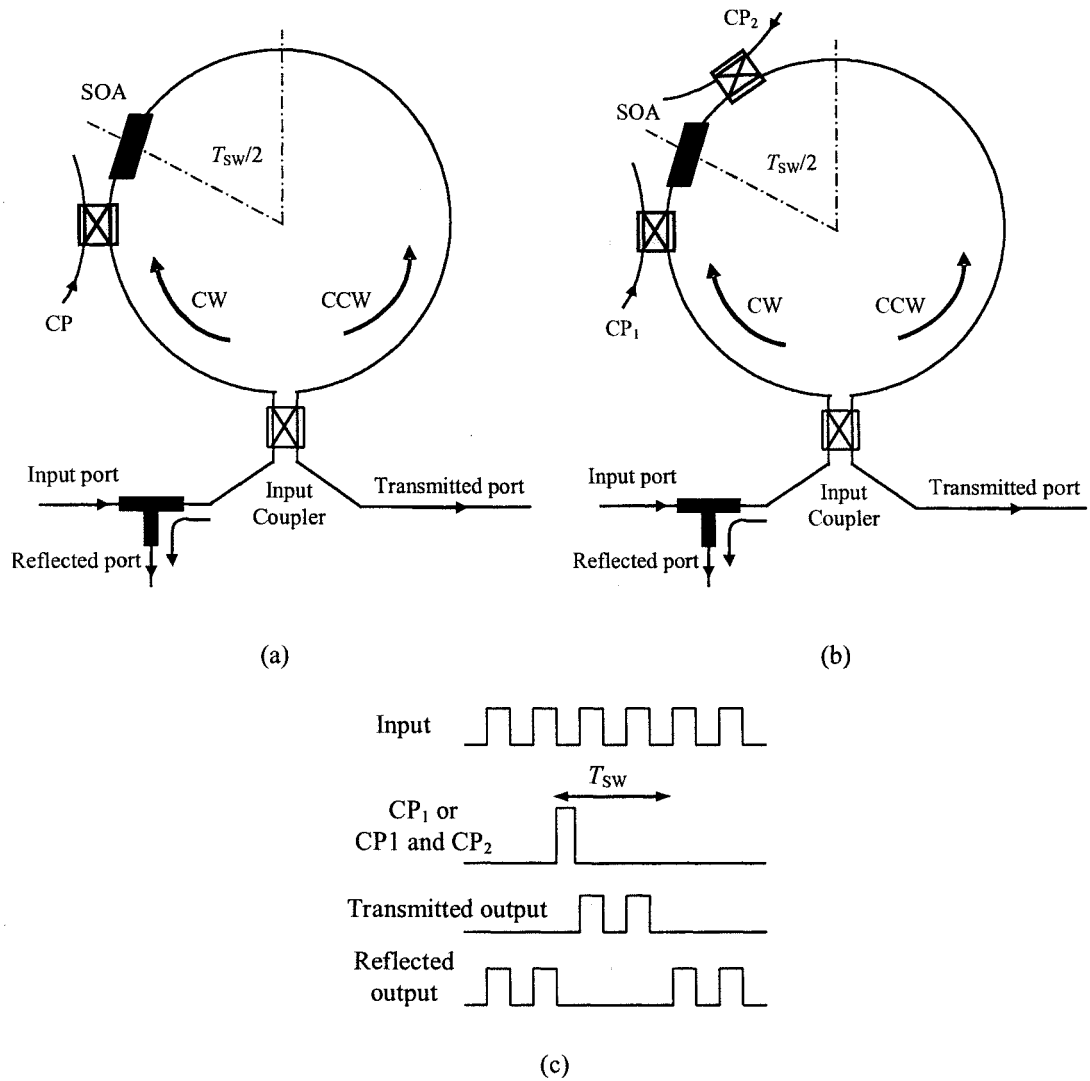
### 3.3 TOAD Switch with Dual-Control Pulses

It is known that the SOA-based TOAD operates with a single control pulse (CP) resulting in an asymmetric switching window [9, 156, 187] that, in turn, introduces a considerable amount of residual crosstalk ( $RCXT$ ) in high-speed all-optical switching or OTDM demultiplexing employing TOAD. To minimise  $RCXT$  the TOAD SW profile needs to be improved. The use of two cascaded TOADs, where both switching windows are overlapped, will result in a narrow and symmetric SW profile [156]. However the complexity and the requirement of precise setting up of cascading TOADs hinder the TOAD simplicity.

In this thesis, a single TOAD switch with new dual-control-pulses (CPs) scheme will be proposed as an alternative solution to address the above  $RCXT$  issue.

### 3.3.1 TOAD operation principle

The diagrams of TOADs with a conventional single control and proposed dual control pulses are shown in Figure 3.8(a) and (b), respectively. Figure 3.8(c) illustrates the temporal switching process for both TOAD configurations.



**Figure 3.8** TOAD switch with (a) a single control pulse, (b) dual control pulses and (c) temporal TOAD pulse diagram of input, control pulse and output signals

A TOAD is basically constructed using a short optical fibre loop with a SOA positioned in a fixed location offset from the loop centre, which is defined by the offset time  $T_{\text{SW}}/2$ . Data signals entering the TOAD via the input port are split by the input coupler into two components clockwise (CW) and counter-clockwise (CCW). With no control pulse, the CW and CCW components propagating within the loop will experience the same unsaturated amplifier gain  $G_0$ , being recombined at the input coupler and emerge from the reflected port. The input and reflected signals are separated using an optical circulator. Introducing a single CP or dual CPs ( $\text{CP}_1$  and  $\text{CP}_2$ ) into the fibre loop will change the nonlinear properties of the SOA, and as a result, the CW and CCW components will experience different levels of gain and phase. Therefore when being recombined at the input coupler, data will exit from the transmitted port (Tx port), thus switching a particular channel or packet within  $T_{\text{SW}}$ . An expression for the TOAD switching window at the transmitted port is given by [25, 28, 109, 188]:

$$\text{SW}(t) = \frac{1}{4} \left[ G_{\text{CW}}(t) + G_{\text{CCW}}(t) - 2\sqrt{G_{\text{CW}}(t)G_{\text{CCW}}(t)} \cos(\Delta\phi(t)) \right], \quad (3.5)$$

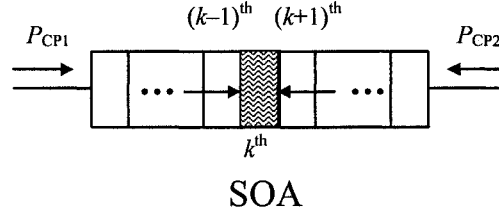
$$\Delta\phi(t) = -0.5\alpha_{\text{LEF}} \ln(G_{\text{CW}}(t)/G_{\text{CCW}}(t)), \quad (3.6)$$

where  $G_{\text{CW}}(t)$  and  $G_{\text{CCW}}(t)$  are the gain profiles of CW and CCW, respectively.  $\Delta\phi(t)$  is the phase difference between  $G_{\text{CW}}(t)$  and  $G_{\text{CCW}}(t)$ .  $\alpha_{\text{LEF}}$  is the SOA linewidth enhancement factor.

The SOA gain is computed by [26, 41, 161]:

$$G(t) = P(L_{\text{SOA}}, t) / P(0, t) = \exp(\Gamma g_d L_{\text{SOA}}), \quad (3.7)$$

where  $L_{\text{SOA}}$  is SOA length. To numerically compute the gain profiles, the SOA is modelled as  $M$  segments (see Figure 3.9) in which the carrier density and the power are spatially approximated for each independent segment.



**Figure 3.9** SOA model composed of  $M$  segments with optical powers entering from both ends

From (3.1), at a time  $t_m$  the change of carrier density  $\Delta N$  in  $\Delta t$  (a time increment for numerical calculation) at segment  $k$  is governed by the SOA rate equation as:

$$\frac{\Delta N(k, t_m)}{\Delta t} = \frac{I_e}{qV_{\text{SOA}}} - \frac{N(k, t_m)}{T_{\text{sp}}} - \frac{P(k, t_m)\Gamma g_d(k, t_m)}{h\nu_0 A_{\text{SOA}}}, \quad (3.8)$$

where  $N(k, t_m)$  and  $P(k, t_m)$  are the carrier density and the optical power at the  $k^{\text{th}}$  segment at the given time  $t_m$ . The segment carrier density depends on the power presence in the segment at the given time. Therefore, the updated carrier density and total power of the segment are given by:

$$N(k, t_m) = N(k, t_{m-1}) + \Delta N(k, t_{m-1}). \quad (3.9)$$

In the case of a single CP, the power at the  $k^{\text{th}}$  segment is from either the  $(k-1)^{\text{th}}$  or  $(k+1)^{\text{th}}$  segment whereas in dual CPs it comprises both powers propagating from the  $(k-$

1)<sup>th</sup> and (k+1)<sup>th</sup> segments. Assuming that a single CP is injected to the loop in the CW direction (see Figure 3.8(a))  $P(k, t_m)$  is given by:

$$P(k, t_m) = P_{CW}(k, t_m), \quad (3.10)$$

and for the dual CP, the segment power is:

$$P(k, t_m) = P_{CW}(k, t_m) + P_{CCW}(k, t_m). \quad (3.11)$$

From (3.7) the incident powers from the CW and CCW directions are computed by:

$$\begin{aligned} P_{CW}(k, t_m) &= P_{CW}(k-1, t_{m-1}) \exp(\Gamma g_d(k-1, t_{m-1}) \Delta L) \\ P_{CCW}(k, t_m) &= P_{CCW}(k+1, t_{m-1}) \exp(\Gamma g_d(k+1, t_{m-1}) \Delta L) \end{aligned} \quad (3.12)$$

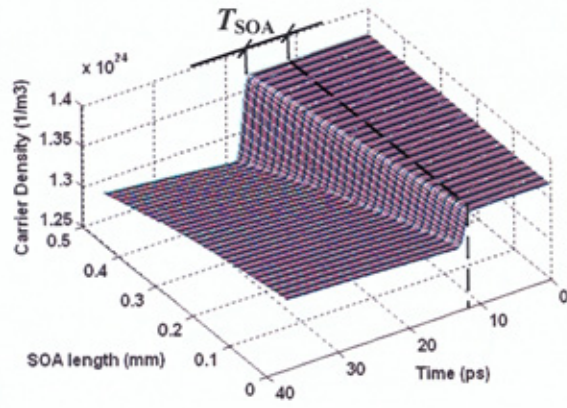
The numerical investigations of SW profiles for TOAD switches with single and dual control pulses are performed by plotting the SOA carrier density changes and gain profiles based on (3.5) - (3.12). The TOAD and SOA parameters are given in Table 3.1 [26, 28, 50].



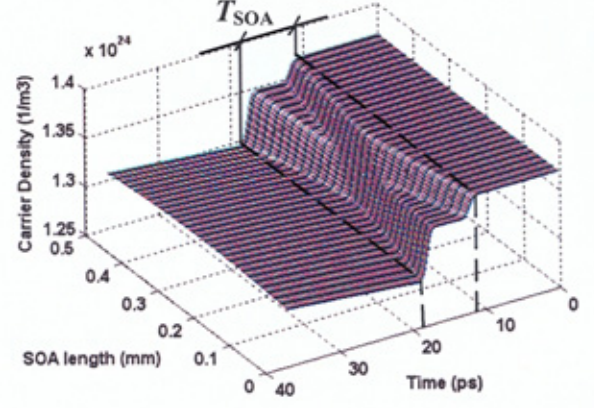
**Table 3.1** TOAD and SOA parameters for switching profile calculation

Parameters	Values
Single CP (peak) power	20 dBm
Dual CP (peak) power (in total)	20 dBm
Control pulse width - FWHM	2 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Number of SOA segments - $M$	200
Switching window width - $T_{sw}$	2 ps
SOA length - $L_{SOA}$	$500 \times 10^{-6}$ m
Confinement factor - $\Gamma$	0.2
Linewidth enhancement factor - $\alpha_{LEF}$	4
Spontaneous emission time - $T_{sp}$	100 ps
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Cross-section area of active region - $A_{SOA}$	$2.4 \times 10^{-13}$ m <sup>2</sup>
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup>
Effective DC injection current - $I_e$	0.15 A
Propagation time - $T_{SOA}$	5.8 ps

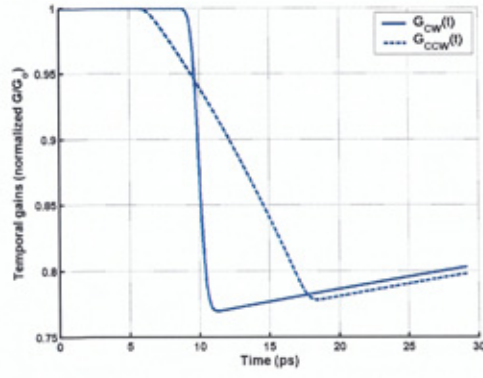
Figure 3.10(a) and (b) show the SOA carrier density changes when it is excited by a single CP and dual CPs, respectively. For a single CP case, the carrier density gradually decreases along the SOA length as CP longitudinally propagates along all segments. This is due to the CP itself being amplified in every segment. As a result, the CW data component following the CP will receive the full SOA saturated gain, thus there is a rapid drop in  $G_{CW}$  level. However, the CCW component, which enters the SOA  $2 \times T_{SOA}$  later than CP where  $T_{SOA}$  is the time for signal propagates through a SOA, will experience partial-longitude saturated SOA gains (at different values). The partial gain level is mainly determined by the locations of both the CP and CCW components within the SOA, which results in a slow reduction in the gain level in  $G_{CCW}$ , see Figure 3.10(c).



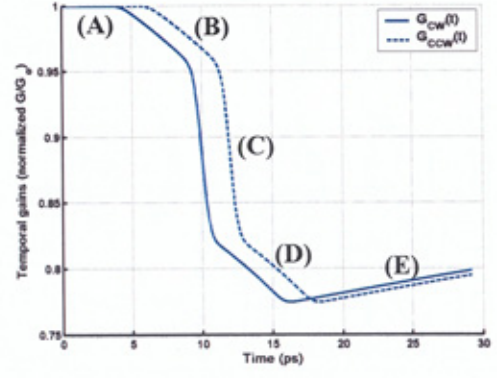
(a)



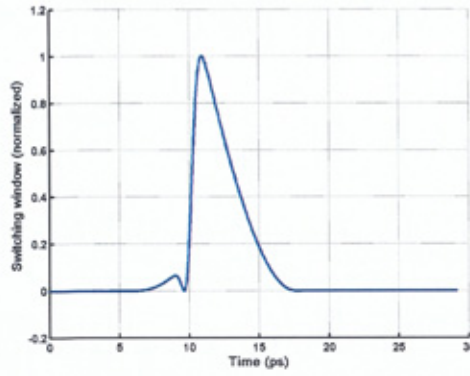
(b)



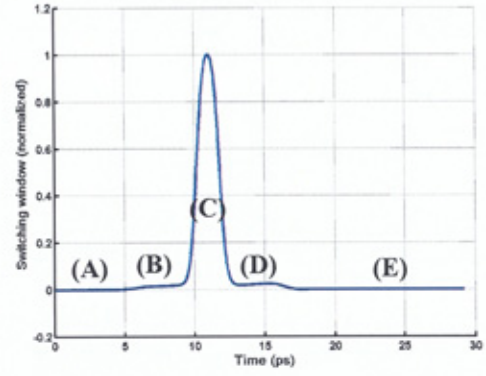
(c)



(d)



(e)



(f)

**Figure 3.10** SOA carrier density changes in (a) single CP and (b) dual CP schemes  $G_{CW}$  and  $G_{CCW}$  in (c) single CP (d) dual CP schemes, and resultant SWs corresponding to (e) single CP and (f) dual CP schemes

In contrast, in the case of dual CPs the segment carrier densities display a symmetrical profile from the SOA centre to its ends, as in Figure 3.10(b). Thus, the gain profiles  $G_{CW}$  and  $G_{CCW}$  would be identical except for the temporal delay  $T_{SW}$ , as in Figure 3.10(d). In region A  $G_{CW}$  and  $G_{CCW}$  are equal to the unsaturated SOA gain  $G_0$ , prior to the CPs being injected into the SOA. With the CPs applied to the SOA just after the CW and before CCW components, the CW and CCW components will experience different SOA gains and phases as outlined below:

- With the  $CP_1$  and  $CP_2$  entering the first and last segments of the SOA, respectively, only parts of CW and CCW components already residing within the SOA are subjected to the gain and phase changes induced by the counter-propagating  $CP_2$  (CCW direction) and  $CP_1$  (CW direction), respectively.  $G_{CW}$  and  $G_{CCW}$ , within the time period  $T_{SOA}$  (time required for a pulse propagating through SOA) in this case, display identical slow responses shown in region B.
- With the CPs having fully propagated through the SOA (i.e.  $CP_1$  and  $CP_2$  arrive at the last and first segments, respectively), the subsequent CW component (in  $T_{SOA}$ ) following  $CP_1$  propagating through the SOA will therefore experience full gain saturation, thus resulting in a rapid level change in the gain profiles, see region C. However, since the CW component also counter-propagates against  $CP_2$  during  $T_{SOA}$ , the gain is further saturated to a new level (i.e. region D).
- With CPs emerging from both ends of the SOA, the SOA gain will start recovering back to its initial state  $G_0$ . CW and CCW components arriving at the SOA during this time will experience the recovery gain characteristic, see region E in Figure 3.10(d).

Figure 3.10(e) and (f) depict narrow switching window profiles with a  $T_{SW}$  of 2 ps for the single and dual CP schemes, respectively. Note that there is an improvement in the SW profile in the dual CP scheme in comparison to that of the conventional single CP case. In Figure 3.10(f), small residual gains outside the SW in regions B and D are due to the slow gain responses in regions B and D in Figure 3.10(d). Figure 3.11 shows a number of TOAD normalised SW profiles with different SW  $T_{SW}$  widths. For  $T_{SW} < T_{SOA}$ , SW gain is relatively small because  $G_{CW}$  and  $G_{CCW}$  are too close, resulting in the relative gain level difference between them being small (see Figure 3.10(d)). Beyond this, the SW gain level is stable.

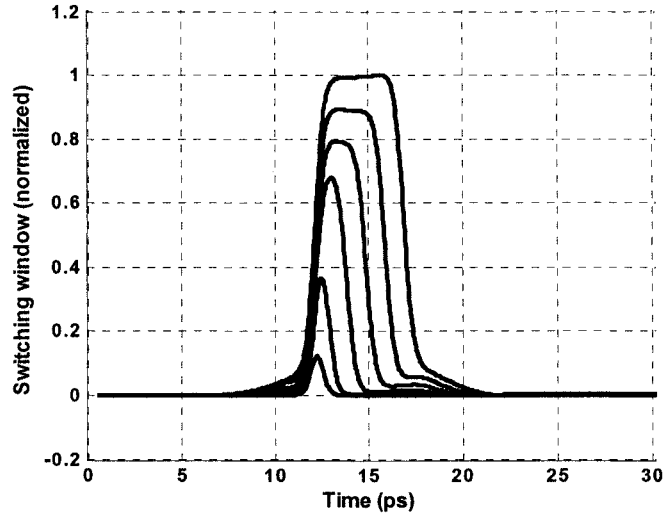


Figure 3.11 TOAD switching windows with different  $T_{SW} = 0.5, 1, 2, 3, 4$  and  $5$  ps

### 3.3.2 Performance analysis

$RCXT$ , BER and the received power penalty  $\Delta P_{rx}$  are the key parameters adopted to assess the TOAD performance. For switching or OTDM demultiplexing,  $\Delta P_{rx}$  is the

power difference between the received power  $P_{rx}$  of baseline rate (back-to-back) and received power  $P_{rx}$  of the switched/demultiplexed OTDM channel.  $RCXT$  and BER analysis of TOADs switching and demultiplexing have been presented in literatures [5, 189-193]. In this section, the essential BER calculation is briefly outlined as the basis for developing and calculating  $P_{rx}$  and  $\Delta P_{rx}$  improvement for the TOAD switch employing the proposed dual-CP scheme.

$RCXT$ , defined as the ratio of  $P_{nt}$  to  $P_t$ , the power of the switched non-target and the switched target signals, respectively, is:

$$RCXT = 10\log_{10}(P_{nt}/P_t), \quad (3.13)$$

and the BER is calculated by [5, 189, 191, 192]:

$$BER = 0.5 \operatorname{erfc}(Q/\sqrt{2}), \quad (3.14)$$

in which, the  $Q$  factor is computed by:

$$Q = (\bar{I}_m - \bar{I}_s) / (\sigma_{t,m} + \sigma_{t,s}), \quad (3.15)$$

where  $\bar{I}_m$  and  $\bar{I}_s$  are the received mean photocurrents for the received mark  $I_m$  and space  $I_s$ .  $\sigma_{t,m}^2$  and  $\sigma_{t,s}^2$  are the total noise powers deteriorating the received mark and space signals. Assuming the probabilities of transmitted mark and space are equal (i.e. 0.5),  $\bar{I}_m$  and  $\bar{I}_s$  are given by:

$$\begin{aligned}\bar{I}_m &= K \times (2P_s) \times (1 + RCXT) \\ \bar{I}_s &= K \times (2P_s) \times (RCXT)\end{aligned}\quad , \quad (3.16)$$

where  $K = \eta_{in} G \eta_{out} L_f R_p$ .  $\eta_{in}$  and  $\eta_{out}$  are the SOA input and output coupling efficiencies, respectively,  $G_{SOA}$  is the SOA gain,  $L_f$  is the optical filter loss,  $R_p$  is the photodetector responsivity and  $P_s$  is the average received signal power without  $RCXT$ . The equivalent amplified spontaneous emission (ASE) current, induced by the SOA, at the receiver is [189, 191]:

$$I_{ASE} = 0.5 NF_{SOA} G_{SOA} \eta_{out} q B_o L_f . \quad (3.17)$$

In (3.17),  $NF_{SOA}$  is the SOA noise figure [194] and  $B_o$  is the optical bandwidth. The noise sources contributing to the deterioration of the signal in OTDM demultiplexing are the relative intensity noise RIN ( $\sigma_{RIN}^2$ ) from the transmitter and TOAD, the ASE of the SOA ( $\sigma_{SOA}^2$ ), the shot noise and the thermal noise of the receiver ( $\sigma_{receiver}^2$ ). The noise variances are given by [5, 189, 191]:

$$\sigma_{RIN,m}^2 = \bar{I}_m^2 RIN_T B_e + (2P_s K)^2 RIN_{TOAD} , \quad (3.18)$$

$$\sigma_{RIN,s}^2 = \bar{I}_s^2 RIN_T B_e , \quad (3.19)$$

$$\sigma_{SOA,x}^2 = 4\bar{I}_x I_{ASE} B_e / B_o + I_{ASE}^2 (2B_o - B_e) / B_o^2 , \quad (3.20)$$

$$\sigma_{receiver,x}^2 = 2q(\bar{I}_x + I_{ASE}) B_e + [4kT_k / R_L + i_a^2] B_e , \quad (3.21)$$

where  $B_e$  is the electrical bandwidth,  $x$  represents mark or space,  $k$  is the Boltzmann constant,  $T_k$  is the temperature (in degrees Kelvin),  $R_L$  is the load resistance of the photodetector and  $i_a^2$  is the power spectral density of the electrical amplifier input noise current.  $RIN_T$  and  $RIN_{TOAD}$  are the relative intensity noise (RIN) of the transmitter and TOAD, respectively.  $RIN_T$  is induced by timing jitters between the electrical modulation signal and the optical pulses (carriers) whereas  $RIN_{TOAD}$  is caused by the combination of timing jitters between the control and signal pulses and due to a non-square SW profile of the TOAD, thus resulting in the intensity fluctuation of switched target signals and hence the switching power penalty.  $RIN_{TOAD}$  is defined in [161, 189]:

$$RIN(\tau) = \frac{V(\tau)}{E^2[w(\tau)]}, \quad (3.22)$$

where  $V(\tau)$  and  $E[w(\tau)]$  are the variance and expected value of target signal energy.  $RIN_{TOAD}$  can be calculated by a given RIN variance  $RMS_{RIN-TOAD}$  [189]. In (3.20), the 1<sup>st</sup> and 2<sup>nd</sup> terms represent the beat noise between the signal and ASE (*sig-ase*), and between ASE and ASE components (*ase-ase*). Assuming that all noises conform to the Gaussian approximation [191, 195], the total noise variance is:

$$\sigma_{t,x}^2 = \sigma_{RIN,x}^2 + \sigma_{SOA,x}^2 + \sigma_{receiver,x}^2. \quad (3.23)$$

The received power penalty of a TOAD is evaluated by computing the optical receiver sensitivity (or the minimum received power  $P_{rx}$  at  $BER = 10^{-9}$ , i.e.  $Q = 6$ ) and comparing it with the  $P_{rx}$  in the back-to-back case. From (3.16):

$$\bar{I}_m - \bar{I}_s = 2KP_s. \quad (3.24)$$

From (3.20), for high  $RCXT$  (i.e. TOAD with single CP),  $sig-ase$  is the dominant term in comparison to the others in (3.18) - (3.21), thus:

$$\begin{aligned}\sigma_{t,m}^2 &= 8KP_s(1 + RCXT_S)I_{ASE}B_e / B_o \\ \sigma_{t,s}^2 &= 8KP_s(RCXT_S)I_{ASE}B_e / B_o\end{aligned}\quad (3.25)$$

Therefore,  $Q$  is expressed by:

$$Q = \frac{2KP_s}{\sqrt{8KP_s(1 + RCXT_S)I_{ASE}B_e / B_o} + \sqrt{8KP_s(RCXT_S)I_{ASE}B_e / B_o}}. \quad (3.26)$$

From (3.26) and  $P_{rx} = P_s(1 + RCXT_S)$ , where  $RCXT_S$  denotes the residual crosstalk in the TOAD with a single CP, the  $P_{rx,S}$  is computed by:

$$P_{rx,S} = \frac{2Q^2B_e}{KB_o}I_{ASE}(1 + RCXT_S)\left(1 + 2RCXT_S + \sqrt{RCXT_S(1 + RCXT_S)}\right). \quad (3.27)$$

With low  $RCXT_D$  (in a TOAD with dual CP), the dominant noise term is the beat noise of the received mark (i.e.  $\sigma_{t,m}^2$ ). Thus,  $Q$  and  $P_{rx,D}$  are calculated by:

$$Q = \frac{2KP_s}{\sqrt{8KP_s(1 + RCXT_D)I_{ASE}B_e / B_o}}, \quad (3.28)$$

$$P_{rx,D} = \frac{2Q^2B_e}{KB_o}I_{ASE}(1 + RCXT_D)^2. \quad (3.29)$$

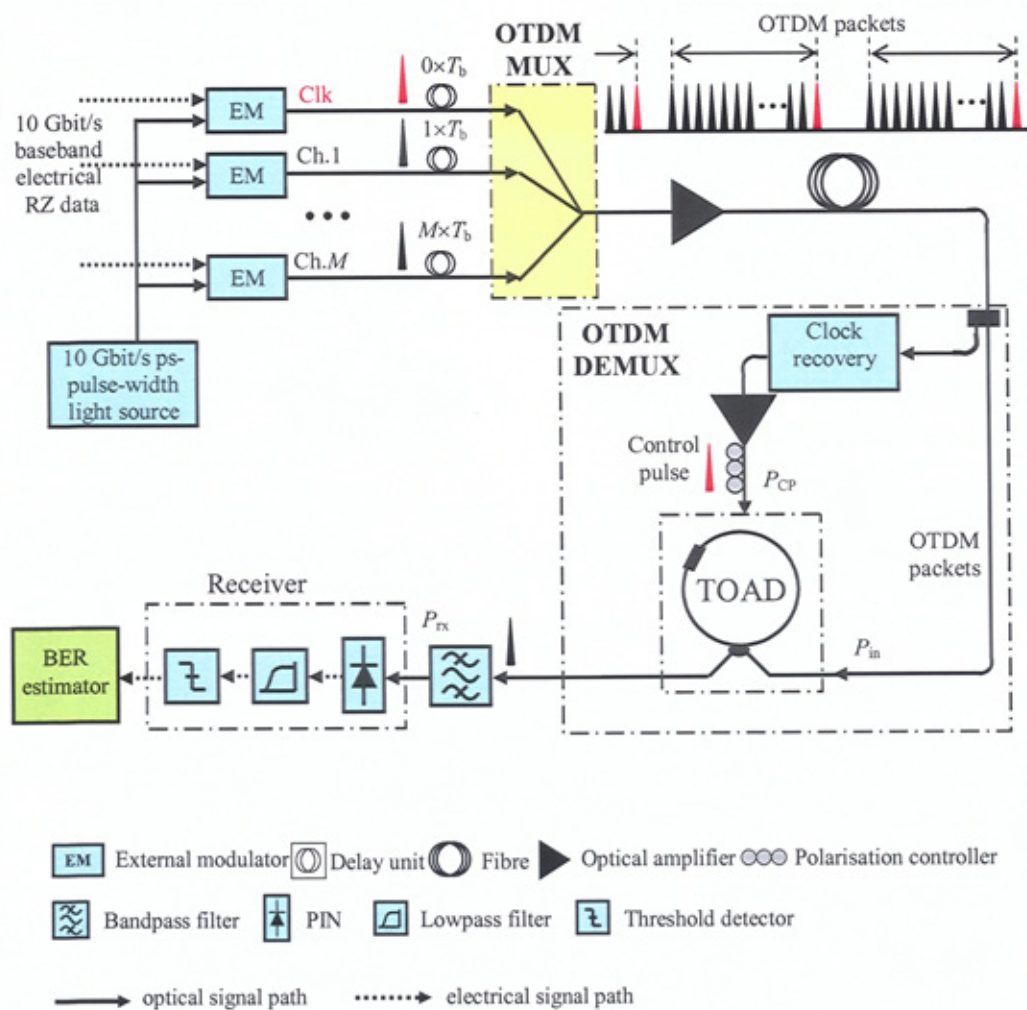
The received power penalty improvement, therefore, will be obtained by:

$$\Delta P_{rx} = P_{rx,D} - P_{rx,S}. \quad (3.30)$$



### 3.3.3 Evaluations, results and discussions

Figure 3.12 shows a typical setup for an OTDM transmission system employing a TOAD as the demultiplexer. The OTDM system comprises of an OTDM transmitter, multiplexer (OTDM-MUX), an optical fibre link, a TOAD demultiplexer, an optical receiver and a BER estimator.



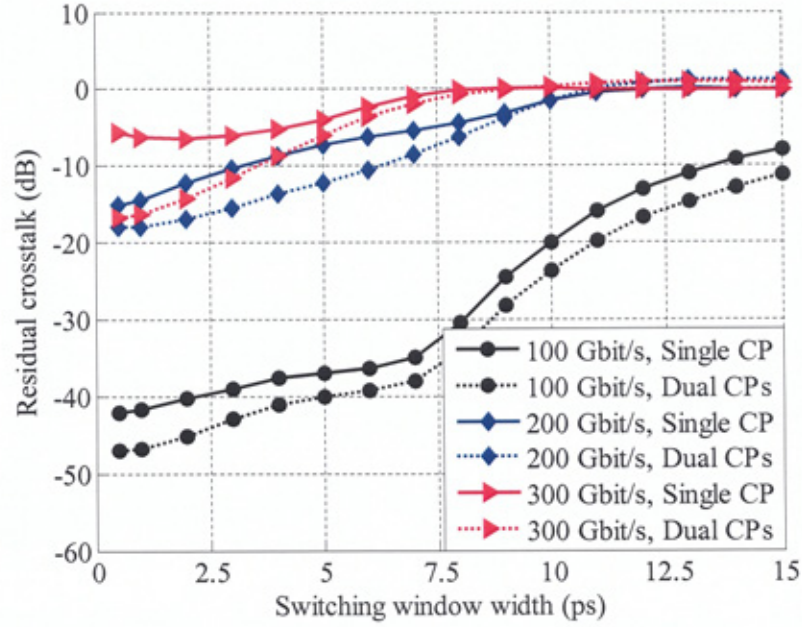
**Figure 3.12** The block diagram of a typical OTDM system and TOAD-based demultiplexer

The transmitted OTDM packet is composed of a clock channel, i.e. a single bit “1” for demultiplexing synchronisation and  $M$  modulated 10-Gbit/s data channels. At the OTDM demultiplexer, the clock bit is recovered using an asynchronous self-clock-recovery unit as proposed in Chapter 6, which is used as a control pulse to drive the TOAD demultiplexer. The output of the demultiplexer is applied to the optical receiver to convert to an electrical signal for BER estimation. The demultiplexed signal is passed through an optical bandpass filter to reduce the SOA spontaneous-spontaneous noise prior to signal detection by a PIN diode. Finally, a BER estimator is utilised to estimate the BER performance of the demultiplexed signal and the power penalty induced by the TOAD.

For evaluating the proposed dual CP scheme,  $RCXT$ , BER and  $\Delta P_{rx}$  performance of the TOAD demultiplexer are numerically calculated for both control schemes for an OTDM system with aggregate bit rates of 100, 200 and 300 Gbit/s. The calculations are expressed in (3.13) - (3.30). All the important parameters used for calculation are given in Table 3.2. Main SOA parameters for calculation were given in Table 3.1.

**Table 3.2** OTDM and TOAD parameters for BER calculation

Parameters	Values
OTDM aggregate bit rates	100, 200, 300 Gbit/s
Baseline bit rate	10 Gbit/s
Data pulse (peak) power	3 dBm
Single CP (peak) power	26.7 dBm
Dual CP (peak) power (in total)	26.7 dBm
Data and CP width - FWHM	2 ps
Switching window width - $T_{sw}$	4 ps
Optical filter loss - $L_f$	- 2 dB
Optical bandwidth - $B_o$	300 GHz
Electrical bandwidth - $B_e$	$0.7 \times 10$ GHz
Load resistance - $R_L$	50 $\Omega$
Photodetector responsivity - $R_p$	1 A/W
Power spectral density - $i_a^2$	10 pA/Hz <sup>1/2</sup>
RIN variance of TOAD - $RMS_{RIN-TOAD}$	0.5 ps
RIN of transmitter - $RIN_T$	- 20 dB
SOA gain - $G_{SOA}$ (excluding coupling efficiency)	30 dB
Input coupling efficiency - $\eta_{in}$	- 2 dB
Output coupling efficiency - $\eta_{out}$	- 2 dB
SOA noise figure - $NF_{SOA}$	6 dB
(SOA inversion parameter - $n_{sp}$ )	(2)

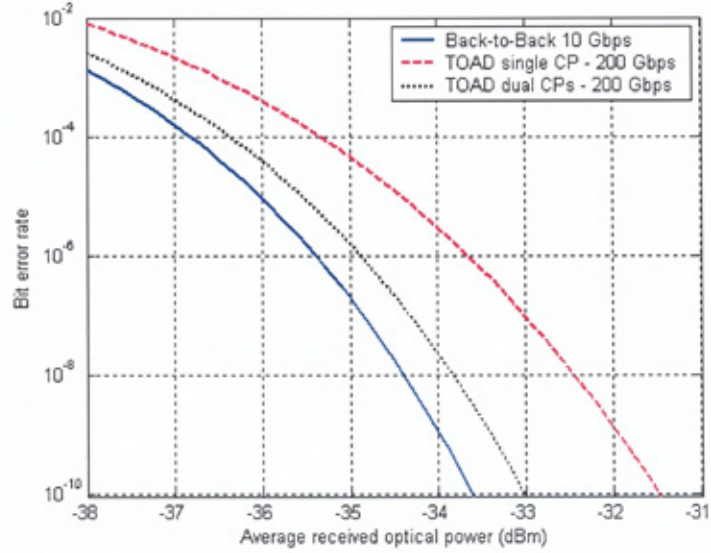


**Figure 3.13** TOAD residual crosstalk  $RCXT$  against the switching window width  $T_{SW}$

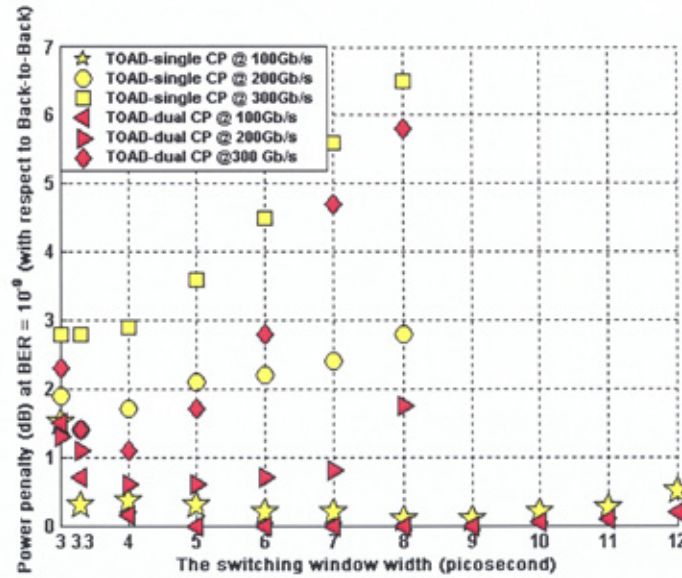
Figure 3.13 shows the calculated  $RCXT$  with respect to  $T_{SW}$  for both CP mechanisms. As expected,  $RCXT$  increases with bit rates because of the asymmetrical SW profile where the trailing-end captures a number of non-target channels with short bit durations  $T_b$  (e.g.  $T_b = 5$  and  $3.3$  ps for the bit rates of 200 and 300 Gbit/s, respectively). However, with dual CP,  $RCXT$  is reduced by 5 dB for SWs of 5 and 3.3 ps corresponding to the demultiplexing of 200 and 300 Gbit/s in comparison to a single-CP. The increase of  $T_{SW}$  leads to the degrading of  $RCXT$  performance since a longer  $T_{SW}$  will allow more non target signals to invade the desired target signal.

The impact of  $RCXT$  is best seen on the BER performance illustrated in Figure 3.14(a). For demultiplexing of 200-to-10 Gbit/s, at BER of  $10^{-9}$  power penalties are 0.6 dB and 2.1 dB (i.e. improvement of 1.5 dB) for dual and single CP cases, respectively,

compared to back-to-back. The received power penalty  $\Delta P_{rx}$  versus switching window width  $T_{sw}$  for a range of higher data rates is shown in Figure 3.14(b).



(a)



(b)

**Figure 3.14** The calculated results of (a) BER for 200-to-10 Gbit/s demultiplexer,  $T_{sw} = 4ps$ , and (b) the received power penalty  $\Delta P_{rx}$  versus different  $T_{sw}$  for different demultiplexing bit rates

The received power penalty is almost flat for both cases at 100 Gbit/s, with the dual CP showing marginal improvement, whereas for higher data rates (200 and 300 Gbit/s)  $\Delta P_{rx}$  improvement is higher by about 1.5 dB for 200 Gbit/s and 300 Gbit/s at SWs of 5 and 3.3ps, respectively. For dual CP,  $\Delta P_{rx}$  minima observed at low values of  $T_{SW}$  are largely due to the reduced RIN and suppressed  $RCXT$ . For larger  $T_{SW}$ ,  $\Delta P_{rx}$  increases due to the deliberate appearance of the non-target channels within the SW.

Overall, in high-speed OTDM system it has been shown that by introducing the dual CP mechanism the TOAD switching or demultiplexing performance is improved.

### 3.4 Summary

This chapter has reviewed the principle of the SOA and its nonlinearity properties used for high-speed all-optical switches. Three main nonlinearity effects XGM, XPM and FWM were presented. Investigations of XGM and XPM were included in the study of the fundamental TOAD switch employing SOA and optical interferometer. A new 3-input AND gate application based on the FWM effect in a single SOA and its performance investigation were published in paper [A8]. A conventional TOAD switch with single CP results in an asymmetrical SW profile, thus inducing high  $RCXT$  in switching. The chapter proposed a dual CP scheme using the TOAD which improved the symmetry of its SW profile, thus reducing  $RCXT$  and minimising the BER and power penalty in comparison to that of a TOAD with a single CP. The improved results have been reported in papers [A2], [A23] and [A24].

It was shown that a TOAD switch with dual CPs offers a fast response and narrow SW. However, its  $T_{\text{SW}}$  is fixed by the offset position of the SOA from its loop centre which results in a limitation in achieving different switching window widths using the same TOAD configuration. In Chapter 4, the research will focus on the SMZ switch and its variants in order to achieve a flexible SW width, better  $RCXT$  and high on/off contrast ratio performances.



## CHAPTER 4

### MACH-ZEHNDER OPTICAL SWITCHES

#### 4.1 Introduction

This chapter presents the background to the SMZ and propose a new controlling scheme using a pair of CPs with unequal powers in order to further suppress its *RCXT*. The SMZ is analytically studied and its *RCXT* performance improvement is analysed through theory and simulation work. The chapter next investigates the inter-channel and inter-output on/off contrast ratio performance of the SMZ switch and proposes a new 1×2 Tri-arm Mach-Zehnder (TaMZ) switch which offers an improved contrast ratio performance than the single SMZ by exploiting the coupling of two SMZs sharing a common arm. In addition, a chained symmetric Mach-Zehnder (CSMZ) architecture is developed from the TaMZ which offers a capability of multiple-channel OTDM switching/demultiplexing with low complexity. For the new proposed TaMZ and CSMZ, their operation stabilities and power penalties are analytically investigated and compared with simulation data.



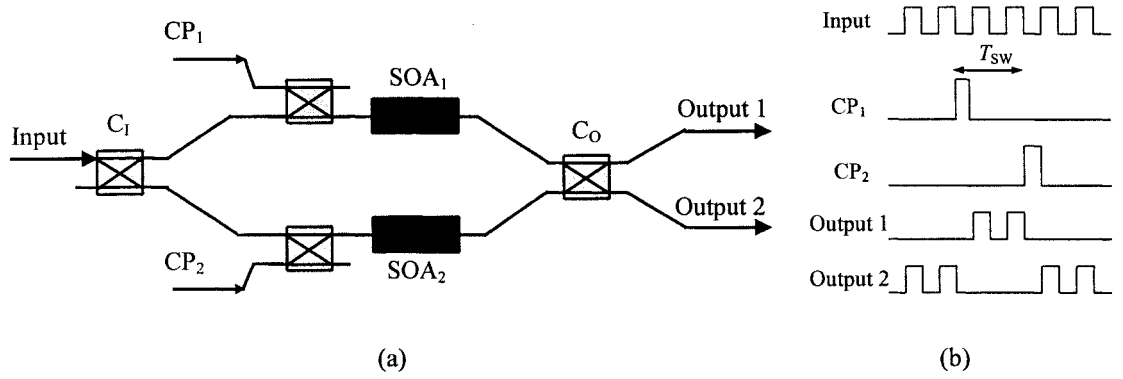
## 4.2 SMZ Switch with Equal and Unequal-Power CPs

A symmetric Mach-Zehnder (SMZ) switch is an alternative to the TOAD to achieve a narrow and symmetric SW with a variable  $T_{SW}$  for use in high-speed OTDM demultiplexing, switching and signal processing applications. In addition, a SMZ offers a much enhanced integration capability as it no longer requires a fibre loop for the interferometer as in a TOAD. SMZ is typically controlled by dual CPs with equal powers when  $T_{SW}$  is narrow (picoseconds) [41, 110, 196]. However, in high-speed optical packet switching applications the requirement for the SW width is in the order of tens of picoseconds or a few nanoseconds, thus a SMZ switch with dual CPs is unsuitable to use because of increased  $RCXT$  at the switched signal. The high  $RCXT$  is due to the mismatched gain profiles of the SMZ arms. In this section, this issue is addressed and a SMZ switch employing CPs with unequal powers is proposed, offering improved  $RCXT$  suppression.

### 4.2.1 SMZ operation principle

A typical SMZ switch comprising an interferometer with two identical arms, SOAs and a number of  $2 \times 2$  couplers is depicted in Figure 4.1(a). The input data signal is fed into the SMZ input via a  $2 \times 2$  coupler  $C_I$ , which introduces a  $\pi/2$  phase shift different between split signals in upper and lower arms. In the absence of the control pulses ( $CP_1$  and  $CP_2$ ), the SMZ is in the balanced state and the data components experience the same gain and phase induced by the SOAs, recombining at the output  $2 \times 2$   $C_O$  coupler and emerging from output port 2 ( $OP_2$ ) whereas no signal emerges from output port 1 ( $OP_1$ ).

This is due to the recombined signals being in-phase and out-of-phase in OP<sub>2</sub> and OP<sub>1</sub>, respectively, when the signals in the upper and lower arms receive a  $\pi/2$  phase shift when they cross C<sub>0</sub> to OP<sub>2</sub> and OP<sub>1</sub>; whereas there is no phase shift being added to these signals when propagating through C<sub>0</sub> to OP<sub>1</sub> and OP<sub>2</sub>.



**Figure 4.1** (a) SMZ switch interferometer configuration and (b) temporal SMZ pulse diagram of input, control and switched signals

In the switching mode both the gain and phase properties of the SOA<sub>1</sub> and SOA<sub>2</sub> are altered by the injection of CP<sub>1</sub> and CP<sub>2</sub> (delayed by a SW duration of  $T_{sw}$ ) via the couplers, respectively, see Figure 4.1(b). This results in SMZ being in an imbalanced state during  $T_{sw}$  and consequently the data signal emerges from OP<sub>1</sub> with no signal at OP<sub>2</sub>. The switching window gain  $SW_1(t)$  and  $SW_2(t)$  of OP<sub>1</sub> and OP<sub>2</sub>, respectively, are computed by [146]:

$$SW_1(t) = \frac{1}{8} \left[ G_1(t) + G_2(t) - 2\sqrt{G_1(t)G_2(t)} \cos(\Delta\phi_{1,2}(t)) \right], \quad (4.1)$$

$$SW_2(t) = \frac{1}{8} \left[ G_1(t) + G_2(t) + 2\sqrt{G_1(t)G_2(t)} \cos(\Delta\phi_{1,2}(t)) \right], \quad (4.2)$$

$$\Delta\phi_{1,2}(t) = -\frac{1}{2}\alpha_{\text{LEF}} \ln\left(\frac{G_1(t)}{G_2(t)}\right), \quad (4.3)$$

where  $G_1(t)$  and  $G_2(t)$  are the temporal gain profiles of SOA<sub>1</sub> and SOA<sub>2</sub> and  $\Delta\phi_{12}(t) = \phi_1 - \phi_2$  is the phase difference between  $G_1(t)$  and  $G_2(t)$ .

Assuming that CP<sub>1</sub> arrives at the SOA<sub>1</sub> before CP<sub>2</sub> at SOA<sub>2</sub>, see Figure 4.1(b), the SOA gain given in (3.7) could be expressed by the total carriers in the longitudinal direction  $z$  of CP propagation along the SOA as:

$$G_1(t) = \exp\left[\int_0^{L_{\text{SOA}}} \Gamma \cdot g_d\left(z, t + \frac{z}{V_g}\right) dz\right], \quad (4.4)$$

$$G_2(t) = \exp\left[\int_0^{L_{\text{SOA}}} \Gamma \cdot g_d\left(z, t + T_{\text{SW}} + \frac{z}{V_g}\right) dz\right], \quad (4.5)$$

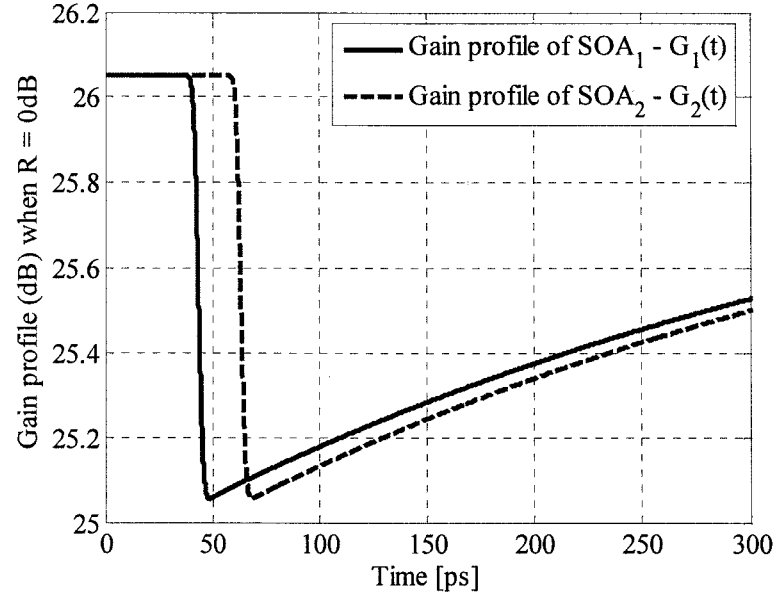
in which  $V_g$  is the group propagation velocity, and  $z/V_g$  is the time increment in the  $z$  direction.

The investigation of temporal gain profiles  $G_1$  and  $G_2$  in SMZ is carried out by mean of calculation in (4.1) - (4.5) with the SMZ and SOA parameters are given in Table 4.1 [26, 28, 50].

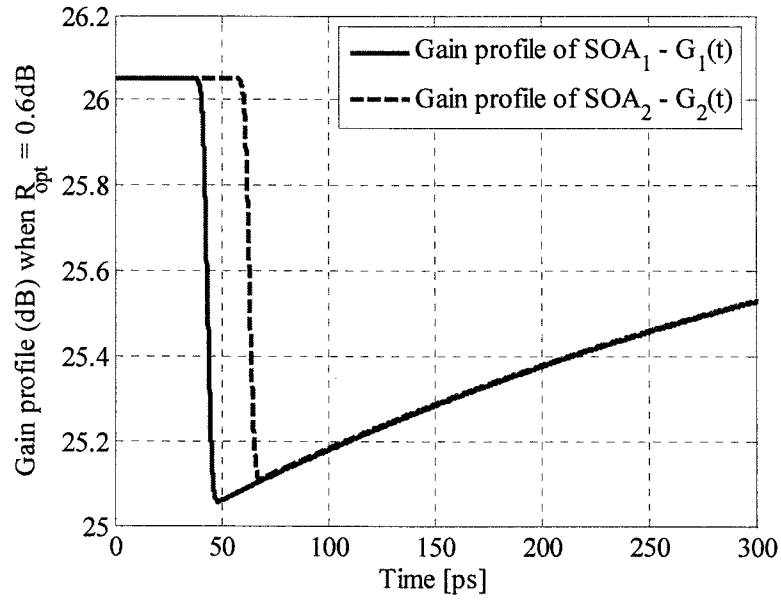
**Table 4.1** SMZ and SOA parameters for gain profile calculation

Parameters	Values
CP <sub>1</sub> (peak) power - $P_{CP1}$	20 dBm
CP <sub>2</sub> (peak) power (equal CP scheme) - $P_{CP2}$	20 dBm
Optimum reduction ratio - $R_{opt}$ (at $T_{SW} = 20$ ps)	0.6 dB
Switching window width - $T_{SW}$	20 ps
Number of segment - $M$	200
SOA length - $L_{SOA}$	$500 \times 10^{-6}$ m
Cross-section area of active region - $A_{SOA}$	$2.4 \times 10^{-13}$ m <sup>2</sup>
Linewidth enhancement factor - $\alpha_{LEF}$	4
Confinement factor - $\Gamma$	0.2
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup> [26]
Spontaneous emission time - $T_{sp}$	100 ps
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Group velocity - $V_g$	$3 \times 10^8$ / 3.5 ms <sup>-1</sup>
Effective DC injection current - $I_e$	0.15 A

Figure 4.2(a) depicts the temporal gain profiles  $G_1$  and  $G_2$  with  $P_{CP1} = P_{CP2} = 100$  mW and a large  $T_{SW} = 20$  ps. With CP<sub>1</sub> applied to SOA<sub>1</sub>,  $G_1$  drops to its saturated level of 25.05 dB. However,  $G_1$  starts to recover back to its un-saturated level of 26.05 dB once CP<sub>1</sub> has exited the SOA<sub>1</sub>. The gain recovery process is rather slow, typically in the range of a few hundreds of picoseconds, being dependent on the SOA properties and the value of  $P_{CP1}$  [26, 41]. After a delay of  $T_{SW}$ , CP<sub>2</sub> is applied to SOA<sub>2</sub> to change the gain profile  $G_2$  in a similar manner to that of SOA<sub>1</sub>.  $G_2$  displays the same characteristic as  $G_1$  except for being delayed by  $T_{SW}$ . Hence, there is a level difference between  $G_1$  and  $G_2$  in the recovery region. This gain difference will induce residual gain outside SW<sub>1</sub> (4.1) due to a non-zero phase difference (4.3), thus resulting in the  $RCXT$  outside the SW<sub>1</sub> (in  $T_{SW}$ ).



(a)



(b)

**Figure 4.2** Temporal gain profiles  $G_1$  and  $G_2$  of SOA<sub>1</sub> and SOA<sub>2</sub>, respectively, in SMZ switch ( $T_{\text{sw}} = 20$  ps) with (a) equal control pulses and (b) unequal control pulses with  $R_{\text{opt}} = 0.6$  dB

Residual crosstalk can be suppressed by limiting the gain saturation level of SOA<sub>2</sub> such that it overlaps with that of SOA<sub>1</sub> in the recovery region. From (3.1) and (4.3) - (4.5), the saturation gain levels of SOAs are monotonously dependent on the excitation powers  $P_{CP1}$  and  $P_{CP2}$ , respectively. Therefore, to match the gain saturation level of SOA<sub>2</sub> with that of SOA<sub>1</sub>, the power in CP<sub>2</sub> should be reduced. The power reduction ratio  $R$  is defined by:

$$R(\text{dB}) = P_{CP1}(\text{dB}) - P_{CP2}(\text{dB}). \quad (4.6)$$

The value of  $R$  depends on the characteristics of the SOA and the CP powers.  $R$  is optimum when  $G_1$  and  $G_2$  overlap in the recovery region, which can be numerically computed by solving (4.4) and (4.5) for a given  $P_{CP1}$  as:

$$\begin{cases} G_2(t, P_{CP2}) = G_1(t + T_{SW}, P_{CP1}) \\ R = \frac{P_{CP1}}{P_{CP2}} \end{cases} \quad (4.7)$$

Figure 4.2(b) displays the gain profiles when employing CPs with unequal powers. It is shown that, at  $R_{\text{opt}}$  of 0.6 dB, both  $G_1$  and  $G_2$  are well matched, thus ensuring the phase difference is zero, which in turn suppresses the *RCXT*.

#### 4.2.2 Performance analysis and results

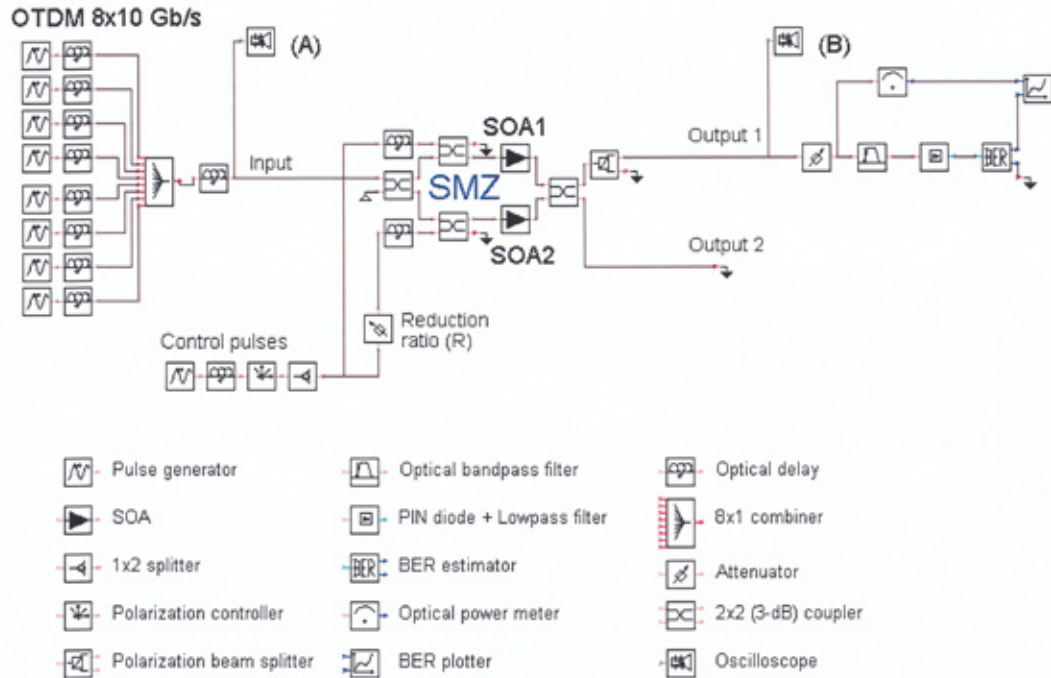
A detailed analysis of the *RCXT* and the BER for an all-optical switch based on the SOA was presented in Section 3.3.2. Similar to (3.27) and (3.29), the received powers for the cases  $R = 0$  (equal control pulses) and  $R_{\text{opt}}$  (optimum unequal control pulses) are derived as the followed:

$$P_{rx, R=0} = \frac{2Q^2 B_e}{KB_0} I_{ASE} (1 + RCXT) \left( 1 + 2RCXT + \sqrt{RCXT(1 + RCXT)} \right), \quad (4.8)$$

$$P_{rx, R_{opt}} = \frac{2Q^2 B_e}{KB_0} I_{ASE} (1 + RCXT_{opt})^2, \quad (4.9)$$

where  $RCXT_{opt}$  is the residual crosstalk determined at  $R_{opt}$ .

The performance of the SMZ switch is evaluated theoretically and by means of simulation using VPI software. Figure 4.3 shows the simulation schematic of an OTDM system consisting of OTDM transmitter, SMZ and an optical receiver, based on the model given in Figure 3.12 where the SMZ replaces the TOAD as the OTDM demultiplexer.



**Figure 4.3** The schematic of BER simulation of OTDM system employing SMZ switch in VPI

The OTDM transmitter is composed of 8×10 Gbit/s channels multiplexed using delay lines (delayed by one bit duration  $T_b = 12.5$  ps) and an 8×1 coupler. The demultiplexed/switched signal (channel) at the SMZ OP<sub>1</sub> is passed through an optical filter before being processed at the optical receiver and the BER estimator. The reduction ratio is set using an optical attenuator placed in the CP<sub>2</sub> arm. The parameters adopted for theoretical calculation and VPI simulation are adopted and shown in Table 4.2 and Table 4.3 [50, 74, 197-199].

**Table 4.2** SOA parameters for BER simulation

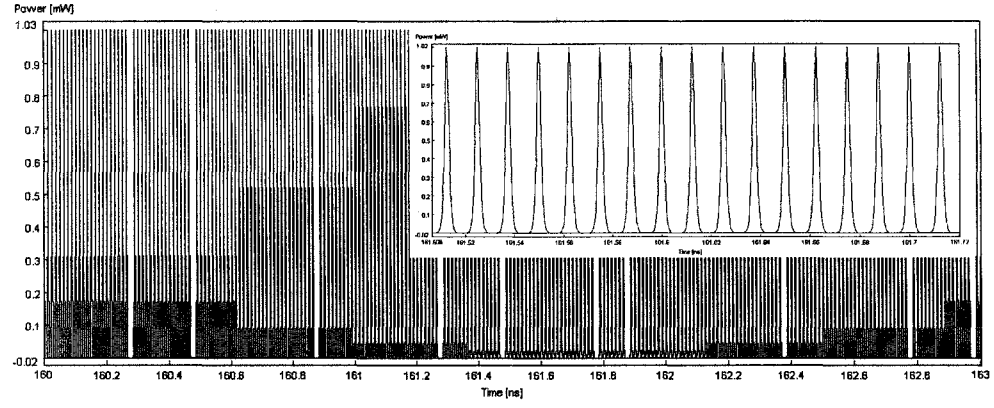
Parameters	Values
SOA gain - $G_{\text{SOA}}$ (excluding coupling efficiency)	30 dB
Input coupling efficiency - $\eta_{\text{in}}$	- 2 dB [199]
Output coupling efficiency - $\eta_{\text{out}}$	- 2 dB
SOA length - $L_{\text{SOA}}$	$500 \times 10^{-6}$ m
SOA active region width	$3 \times 10^{-6}$ m
SOA active region height	$80 \times 10^{-9}$ m
SOA noise figure - $NF_{\text{SOA}}$ (SOA inversion parameter - $n_{\text{sp}}$ )	6 dB (2)
Linewidth enhancement factor - $\alpha_{\text{LEF}}$	4
Confinement factor - $\Gamma$	0.2
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup>
Internal losses	$40 \times 10^2$ m <sup>-1</sup>
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Group velocity - $V_g$	$3 \times 10^8$ / 3.5 ms <sup>-1</sup>
Effective DC injection current - $I_e$	0.15 A
Recombination coefficient A	$1.43 \times 10^8$ s <sup>-1</sup>
Recombination coefficient B	$1 \times 10^{-16}$ m <sup>3</sup> s <sup>-1</sup>
Recombination coefficient C	$3 \times 10^{-41}$ m <sup>6</sup> s <sup>-1</sup>



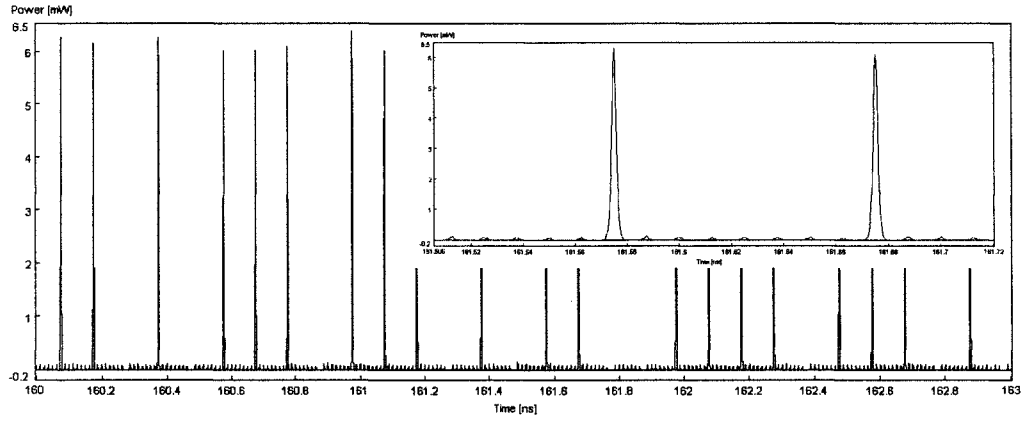
**Table 4.3** OTDM and SMZ parameters for BER simulation

Parameters	Values
OTDM aggregate bit rates	80 Gbit/s
Baseline bit rate	10 Gbit/s
PRBS sequence	$2^{13} - 1$
Data pulse (peak) power	0 dBm (1 mW)
CP <sub>1</sub> (peak) power	10 dBm (10 mW)
Data and CP width - FWHM	2 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Switching window width - $T_{sw}$	10 ps
Optimum reduction ratio - $R_{opt}$ (at $T_{sw} = 20$ ps)	0.6 dB
Optical filter loss - $L_f$	- 2 dB
Optical bandwidth - $B_o$	300 GHz
Electrical bandwidth - $B_e$	$0.7 \times 10$ GHz
Power spectral density - $i_a^2$	10 pA/Hz <sup>1/2</sup>
RIN variance of SMZ - $RMS_{RIN-SMZ}$	0.5 ps
RIN of transmitter - $RIN_T$	- 20 dB
Photodetector responsivity - $R_p$	1 A/W
Load resistance - $R_L$	50 $\Omega$

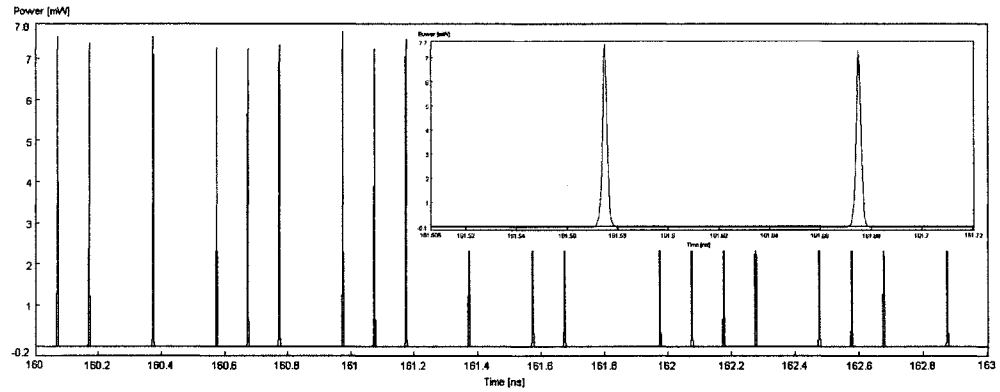
An OTDM pulse train at the input to the SMZ (point (A) in Figure 4.3) is shown in Figure 4.4(a). To demonstrate single channel demultiplexing and assess its BER and power penalty performance, the 3<sup>rd</sup> channel has been selected to have random bits of 0/1 with a  $2^{13}-1$  pseudo random bit sequence (PRBS). Figure 4.4(b) and (c) outline the demultiplexed output pulse train at the probe point (B) for  $R = 0$  dB and  $R = R_{opt} = 0.3$  dB, respectively. The insets in Figure 4.4(a) - (c) are the zoomed waveforms of the OTDM input, demultiplexed signals (for both  $R = 0$  and  $R_{opt}$ ), respectively. Note that the residual *RCXT* is considerably suppressed at  $R_{opt}$ .



(a)



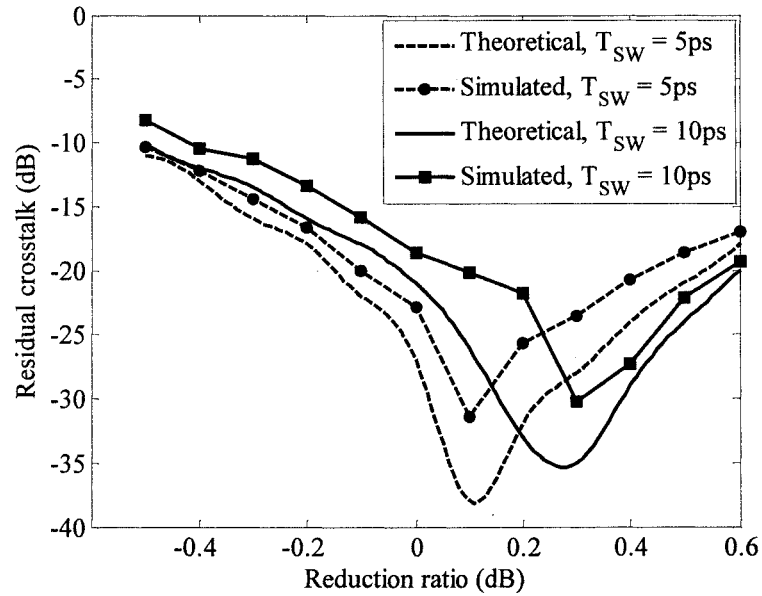
(b)



(c)

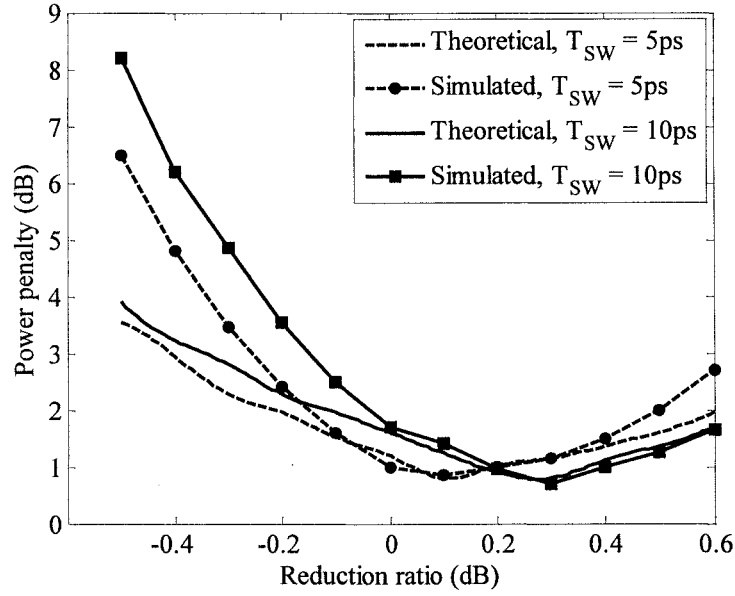
**Figure 4.4** (a) The incoming OTDM pulse stream at the input of SMZ switch - at the point (A) in Figure 4.3 (inset is the zoomed-in version of the pulses), (b) the demultiplexed pulse train from 80Gbit/s-to-10Gbit/s at  $R = 0\text{dB}$  and  $T_{\text{sw}} = 10\text{ ps}$ , the pulses are seen at the point (B), inset shows the demultiplexed pulses and residual crosstalk, and (c) the demultiplexed pulses from 80Gbit/s-to-10Gbit/s at  $R = R_{\text{opt}} = 0.3\text{dB}$ , inset showing the reduction in residual crosstalk.

Predicted (theoretical) and simulated results for the residual crosstalk against the reduction ratio for two different switching window sizes are shown in Figure 4.5. For low values of  $R$ , i.e.  $P_{CP1} < P_{CP2}$ ,  $RCXT$  is relatively high because of the gain difference between  $G_1$  and  $G_2$ .  $RCXT$  decreases with increasing of  $R$ , reaching minimum values at the optimum reduction ratio value of  $R_{opt}$ , before increasing again with high  $R$ . Note the slightly higher simulated  $RCXT$  is explained as follows. In theoretical analysis, the residual power due to non-target channels residing outside the switching window is calculated, whereas in the simulation it is mixed with the noise signal of the demultiplexed channel. For  $T_{SW} = 5$  ps, the predicted and simulated minimum  $RCXT$ s of -37 dB and -31.5 dB are observed at  $R_{opt} = 0.1$  dB. As expected with a wider SW size, the gain difference between  $G_1$  and  $G_2$  is greater, thus requiring larger  $R_{opt}$  to compensate for the gain mismatch.



**Figure 4.5** Theoretical and simulated residual crosstalk  $RCXT$  against reduction ratio  $R$

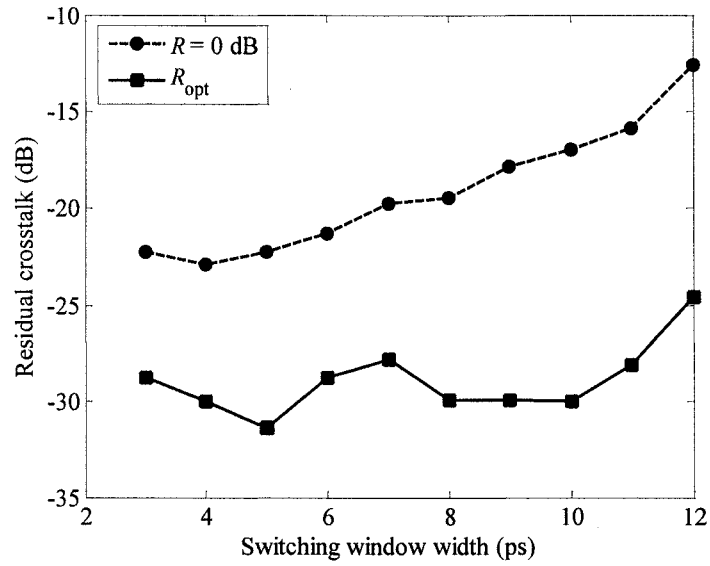
In Figure 4.6, the theoretical and simulated received power penalties against  $R$  for  $T_{SW}$  of 5 and 10 ps are shown. The power penalty also decreases and increases with  $R$ , reaching minimum values of 0.8 dB at  $R = R_{opt}$  for both values of  $T_{SW}$ .



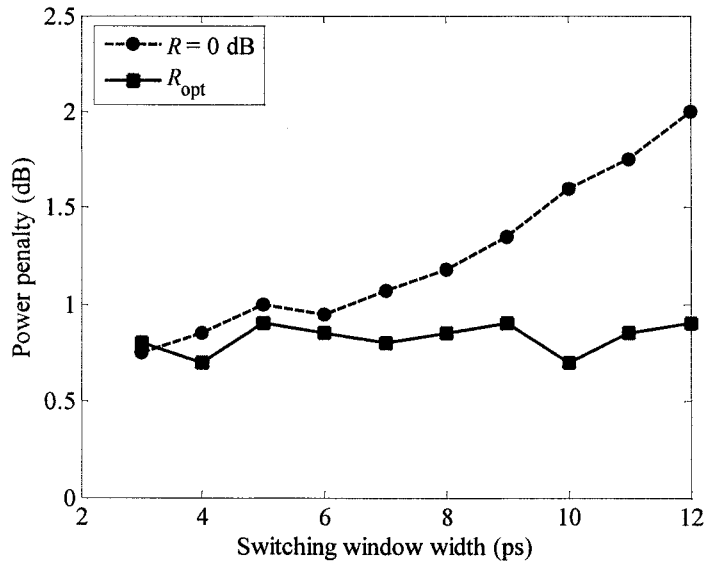
**Figure 4.6** Received power penalty  $\Delta P_{rx}$  against reduction ratio  $R$  for  $T_{SW}$  of 5 ps and 10 ps

The residual crosstalk against SW width for  $R = 0$  and  $R_{opt}$  are next investigated, see Figure 4.7(a). For  $R = 0$  (i.e. equal power control pulses),  $RCXT$  is minimum when  $T_{SW}$  is equal to 4 ps, increasing linearly with  $T_{SW}$ . However, for  $R = R_{opt}$  the  $RCXT$  shows a small variation around the mean value of -30 dB for different values of  $T_{SW}$ . This is because  $G_1$  and  $G_2$  have the same profile in the recovery region.  $RCXT$  will result in power penalties as shown in Figure 4.7(b). Once again for  $R = R_{opt}$  and for all values of  $T_{SW}$ , the power penalty changes very little in comparison to  $R = 0$ . Note for large values

of  $T_{sw}$ , the improvement in the received power penalty is  $> 1$  dB, thus illustrating the potential of the proposed scheme for switching of single as well as multiple channels.



(a)



(b)

**Figure 4.7** Simulated (a) residual crosstalk  $RCXT$  and (b) power penalty of the SMZ switch against the switching window width  $T_{sw}$  for  $R = 0$  and  $R_{opt}$

### 4.3 Tri-arm Mach-Zehnder Switch

The 1×2 TOAD and SMZ switches have been widely utilised for a number of key applications in all-optical high-speed networks such as OTDM demultiplexers [55], logic gates [136], optical flip-flops [149], wavelength conversion [35], 1×2 switching [17] and header processing [143]. In the first four applications, achieving a high on/off contrast ratio ( $CR$ ) between two outputs is not critically required, since only the TOAD transmitted port or SMZ output 1 is used in the switching mode, whereas, in the latter applications, where both outputs are used, a  $CR$  of greater than 20 dB is required for correct operation. However, the typical inter-output  $CR_{OP}$  for the SMZ switch is relatively low ( $\sim 10$  dB) and is sensitive to the controlling scheme and SOA parameter (due to small linewidth enhancement), expressed in (3.5) - (3.7) and (4.1) - (4.3), which consequently results in poor  $CR$  performance.

This section will present a novel 1×2 Tri-arm MZ switch (TaMZ) that achieves higher  $CR$  between two output ports when compared to the conventional SMZ by introducing an auxiliary arm coupled to the two existing arms of the SMZ switch. In addition, a controlling scheme based on a constant signal is proposed, which improves the flatness of the SW gain and the dynamic range of the control signal power. This controlling scheme is similar to an all-optical flip-flop (AOFF).

#### 4.3.1 On/off contrast ratio issues

The SMZ switching windows  $SW_1$  and  $SW_2$  are expressed in (4.1) and (4.2) for  $OP_1$  and  $OP_2$ , respectively. Note that the gains of  $SW_1$  and  $SW_2$  are inversely proportional, and in the normal mode (i.e. without CPs) the input signal is switched to  $OP_2$ . To evaluate the switching performance during the switching period, the following two  $CR$ s required investigating:

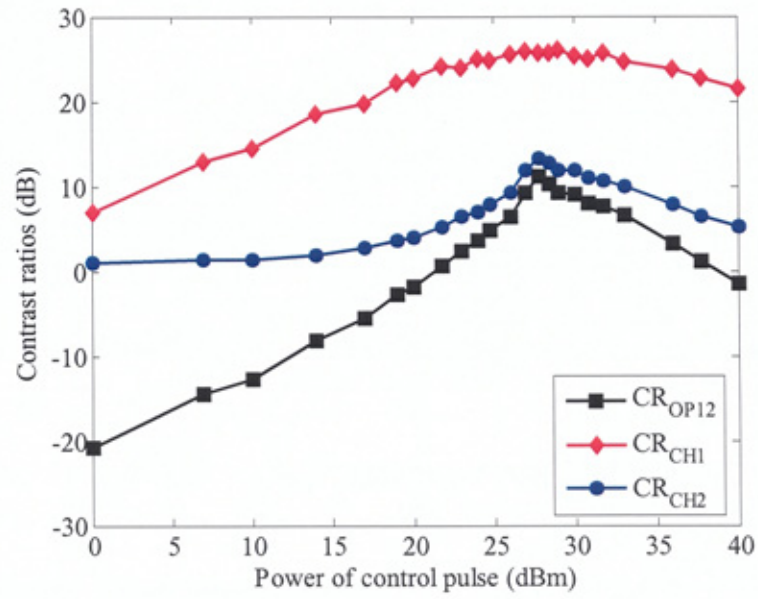
- (i) the inter-output  $CR_{OPij}$ , defined as the power ratio between the switched and non-switched signal at  $OP_i$  and  $OP_j$  ( $i \neq j = 1$  or  $2$ ), respectively, when TaMZ is designed to switch data to  $OP_i$
- (ii) the inter-channel  $CR_{CHi}$ , defined as the power ratio between the switched and non-switched signals at the  $i^{\text{th}}$  output, which are given by:

$$CR_{OPij} = \frac{SW_{i,ON}(t_0 < t < t_0 + T_{SW})}{SW_{j,OFF}(t_0 < t < t_0 + T_{SW})}, \quad (4.10)$$

$$CR_{CHi} = \frac{SW_{i,ON}(t_0 < t < t_0 + T_{SW})}{SW_{i,OFF}(t \notin [t_0, t_0 + T_{SW}])}, \quad (4.11)$$

where  $t_0$  denotes the start of the switching duration  $T_{SW}$ . In (4.10),  $CR_{OP12} \rightarrow 0$  when  $\Delta\phi_{12}(t) = 0$ , i.e.  $G_1 = G_2$  whereas  $CR_{OP12} \rightarrow \infty$  when  $\Delta\phi_{12}(t) = \pi$ . However, to achieve a phase difference of  $\pi$  as in (4.3), the gain difference between  $G_1$  and  $G_2$  and  $\alpha_{LEF}$  needs to be high [41], which requires a high-powered CP and a SOA having a high  $\alpha_{LEF}$ . The graph in Figure 4.8 shows the  $CR$ s against the CP power obtained by simulation using

the SOA parameters given in Table 4.4 (Note that the selected  $\Gamma$  is high to provide high gain for a long packet switching).



**Figure 4.8** Plots of SMZ switching contrast ratios against the control pulse powers with  $T_{sw} = 0.1$  ns



**Table 4.4** SMZ and SOA parameters for CR simulation

Parameters	Values
Data pulse (peak) power	0 dBm
Data and CP width - FWHM	2 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Switching window width - $T_{sw}$	100 ps
SOA length - $L_{SOA}$	$500 \times 10^{-6}$ m
SOA active region width	$2.5 \times 10^{-6}$ m
SOA active region height	$40 \times 10^{-9}$ m
Confinement factor - $\Gamma$	0.5
Linewidth enhancement factor - $\alpha_{LEF}$	4
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup>
Internal losses	$40 \times 10^2$ m <sup>-1</sup>
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Group velocity - $V_g$	$3 \times 10^8$ / 3.5 ms <sup>-1</sup>
Effective DC injection current - $I_e$	0.15 A
Recombination coefficient A	$1.43 \times 10^8$ s <sup>-1</sup>
Recombination coefficient B	$1 \times 10^{-16}$ m <sup>3</sup> s <sup>-1</sup>
Recombination coefficient C	$3 \times 10^{-41}$ m <sup>6</sup> s <sup>-1</sup>

$CR_{OP12}$  and  $CR_{CH2}$  reach the maximums of 12 dB and 13.5 dB, respectively, which are observed at the optimum CP peak power of 28 dBm, and decreasing for all other values of CP power over a wide range due to the inverse proportionality property of (4.1) and (4.2).  $CR_{CH1}$  is higher than  $CR_{CH2}$  with a maximum value of 25 dB at its optimum CP power of 28 dBm due to insufficient  $\alpha_{LEF}$  for  $\Delta\phi_{1,2} \rightarrow \pi$ . In addition, a higher value of  $CR_{CH1}$  is achieved over a wider range than in  $CR_{CH2}$ . This is due to the fact that achieving a zero denominator in (4.11) is easier for  $CR_{CH1}$ , since one needs to set the equality of  $G_1$  and  $G_2$ . On the other hand, maximum value of  $CR_{CH2}$  can be achieved only when setting  $\Delta\phi_{1,2} \rightarrow \pi$ . Note that the decrease in CRs beyond the optimum CP

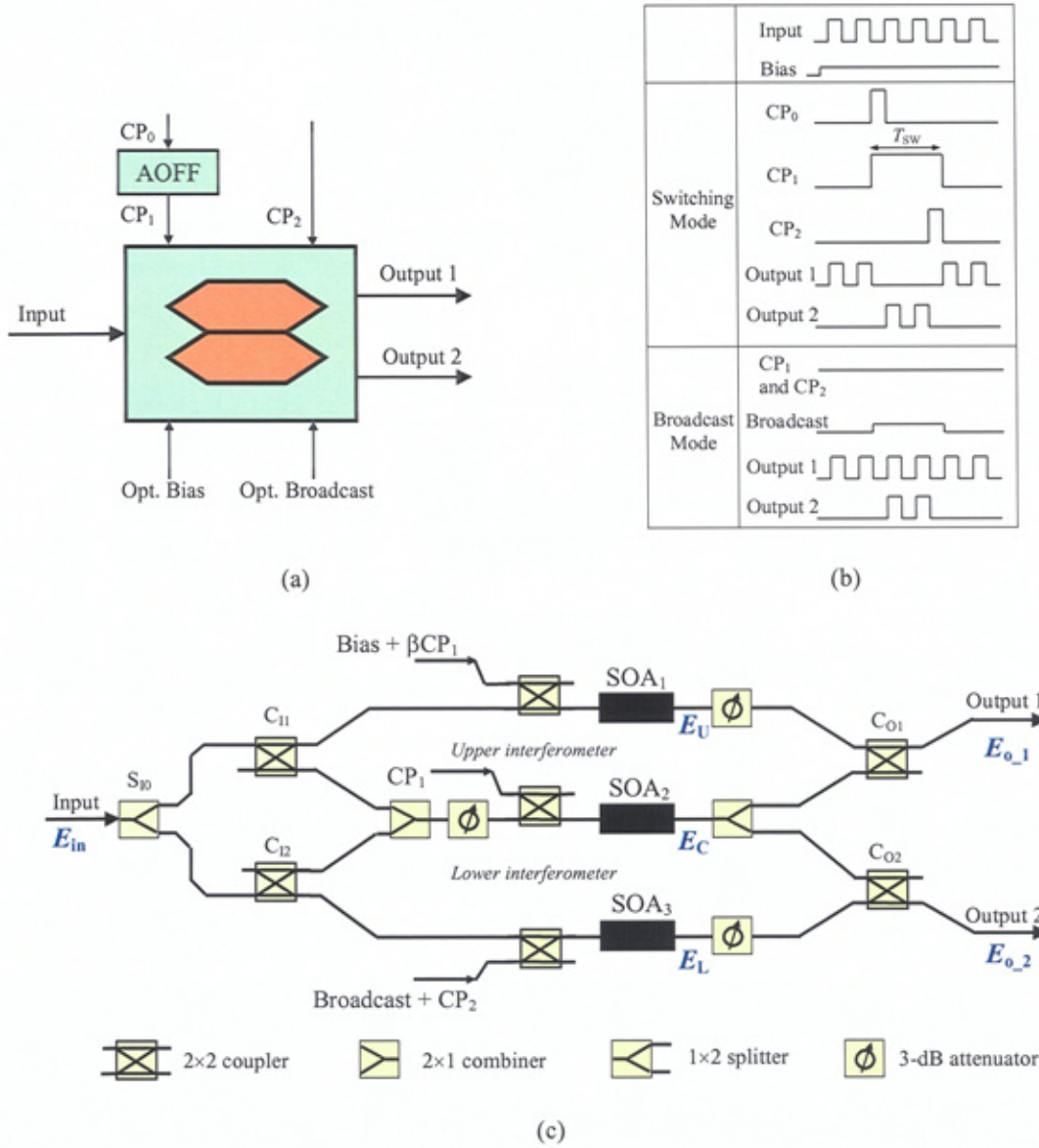
power is due to the low gain difference between  $G_1$  and  $G_2$  and the over saturated SOA gain, thus resulting in reduced input signal amplification.

Since the SMZ  $OP_1$  offers much improved CR in comparison to  $OP_2$ , it is advantageous to couple two SMZs to form a new  $1 \times 2$  TaMZ switch with high CRs at both  $OP_1$  and  $OP_2$ . In addition, the use of AOFF to generate a CP with long pulse duration, instead of using a short CP, will overcome the SOA relaxation time, thus providing capability to switch a long packet (i.e. a large  $T_{sw}$ ). In the following section, a TaMZ-based switch with AOFF is derived and analysed.

#### 4.3.2 TaMZ operation principle

The proposed TaMZ-based  $1 \times 2$ -switch block diagram is depicted in Figure 4.9(a), with an AOFF, an optical bias signal, an optical broadcast signal and two CPs ( $CP_0$  and  $CP_2$ ). The switch operation is illustrated in Figure 4.9(b) for both switching and broadcasting modes. In the normal operation mode with no CPs, a small constant optical bias signal establishes an imbalanced state between the upper and the centre arms (the upper interferometer) of the TaMZ, see Figure 4.9(c). As a result, the input signal emerges from the  $OP_1$  and with no signal at the  $OP_2$ , since the lower interferometer (centre and lower arms) is in the balanced state. In the switching mode,  $CP_0$  is applied to the AOFF to generate a  $CP_1$  (constant power in a duration of  $T_{sw}$ ), which is injected into the upper and centre arms, swapping the current states of the upper and lower interferometers into balanced and imbalanced states, respectively. Therefore,  $OP_1$  is turned off and the input signal emerges from  $OP_2$ . By applying  $CP_2$  to the TaMZ, the gain of  $SOA_3$  is saturated

with its gain and phase profiles matching that of SOA<sub>2</sub>. Therefore the balanced state is restored in the lower interferometer and consequently OP<sub>2</sub> is turned off. At the same time, CP<sub>1</sub> exits SOA<sub>1</sub> and SOA<sub>2</sub>, and, with the upper interferometer in an imbalanced state due to the optical bias signal, OP<sub>1</sub> once again is turned on.



**Figure 4.9** (a) TaMZ-based switch with an AOFF, (b) temporal TaMZ pulse diagram of input, control and switched pulses and (c) TaMZ interferometer configuration

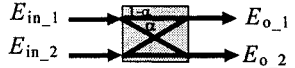
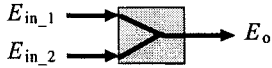
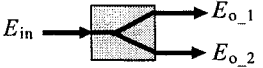
When the optical broadcast signal is applied to the TaMZ, the input signal is switched to both OP<sub>1</sub> and OP<sub>2</sub>. In Figure 4.9(b), when both CP<sub>0</sub> and CP<sub>2</sub> are off whilst the broadcast signal is non-zero, an input packet is switched to both OPs, because both upper and lower interferometers are in an imbalanced state. To completely block the input signal emerging from both switch outputs, only bias and broadcast signals should be applied to ensure the balanced states in both upper and lower interferometers, thus offering additional switching features when compared with the standard SMZ switch.

In the TaMZ configuration, a number of 3-dB attenuators are used to ensure equal power levels at the 2×2 C<sub>O1</sub> and C<sub>O2</sub> couplers. The combination factor  $\beta$  ( $< 1$ ) with CP in the upper arm is used to ensure power equality for both (bias +  $\beta$ CP<sub>1</sub>) and CP<sub>1</sub> signals, thus achieving an ideal balanced state in the upper interferometer when CP<sub>1</sub> is applied. Assuming that the coupler, combiner and splitter are designed with the transfer functions given in Table 4.5, and the input signal has an electrical field  $E_{in}$  [28], the fields in the upper, centre and lower arms after propagating through the SOAs are given by:

$$\begin{aligned}
 E_U &= \frac{1}{2} a_1 e^{-j\phi_1} (1 - \alpha_{11})^{\frac{1}{2}} E_{in} \\
 E_C &= j \frac{1}{4} a_2 e^{-j\phi_2} \left( \alpha_{11}^{\frac{1}{2}} + \alpha_{12}^{\frac{1}{2}} \right) E_{in} , \\
 E_L &= \frac{1}{2} a_3 e^{-j\phi_3} (1 - \alpha_{12})^{\frac{1}{2}} E_{in}
 \end{aligned} \tag{4.12}$$

where  $a_i$  and phase  $\phi_i$  are the field gain and phase, respectively, of a SOA<sub>*i*</sub> complex-gain induced on the electrical field of signal propagating through it.  $\alpha$  is the coupling factor of the 2×2 coupler.

**Table 4.5** Transfer functions of 2×2 coupler, 2×1 combiner and 1×2 splitter

	2×2 coupler	2×1 combiner	1×2 splitter
Schematic			
Transfer function	$\begin{bmatrix} E_{o\_1} \\ E_{o\_2} \end{bmatrix} = \begin{bmatrix} (1-\alpha)^{1/2} & j\alpha^{1/2} \\ j\alpha^{1/2} & (1-\alpha)^{1/2} \end{bmatrix} \begin{bmatrix} E_{in\_1} \\ E_{in\_2} \end{bmatrix}$	$E_o = \frac{1}{\sqrt{2}}(E_{in\_1} + E_{in\_2})$	$E_{o\_1} = E_{o\_2} = \frac{E_{in}}{\sqrt{2}}$

From (4.12) and Figure 4.9(c), the output fields at OP<sub>1</sub> and OP<sub>2</sub> are computed as:

$$E_{o\_1} = \frac{E_{in}}{\sqrt{8}} [K_{11}a_1e^{-j\phi_1} - K_{12}a_2e^{-j\phi_2}]$$

$$E_{o\_2} = \frac{E_{in}}{\sqrt{8}} [K_{21}a_3e^{-j\phi_3} - K_{22}a_2e^{-j\phi_2}]$$
(4.13)

with the coefficients  $K_{ij}$  given by:

$$K_{11} = (1-\alpha_{11})^{1/2}(1-\alpha_{01})^{1/2}; \quad K_{12} = \frac{1}{2}(\alpha_{11}^{1/2} + \alpha_{12}^{1/2})\alpha_{01}^{1/2}$$

$$K_{21} = (1-\alpha_{12})^{1/2}(1-\alpha_{02})^{1/2}; \quad K_{22} = \frac{1}{2}(\alpha_{11}^{1/2} + \alpha_{12}^{1/2})\alpha_{02}^{1/2}$$
(4.14)

As the result, the SW gains of OP<sub>1</sub> and OP<sub>2</sub> are found as:

$$SW_1 = P_{o\_1}/P_{in} = (E_{o\_1}E_{o\_1}^*)/(E_{in}E_{in}^*) = \frac{1}{8}[K_{11}^2G_1 + K_{12}^2G_2 - 2K_{11}K_{12}\sqrt{G_1G_2}\cos\Delta\phi_{1,2}],$$
(4.15)

$$SW_2 = P_{o\_2}/P_{in} = (E_{o\_2}E_{o\_2}^*)/(E_{in}E_{in}^*) = \frac{1}{8}[K_{21}^2G_3 + K_{22}^2G_2 - 2K_{21}K_{22}\sqrt{G_3G_2}\cos\Delta\phi_{2,3}], \quad (4.16)$$

where  $\Delta\phi_{i,i+1}$  ( $i = 1, 2$ ) is derived from (4.3) and the power gain  $G$  relates to the signal field gain  $a$  given by [28]:

$$G = a^2. \quad (4.17)$$

Note in (4.15) and (4.16), the on/off states of both outputs only depend on the gain-level equalities of  $G_1$ ,  $G_2$  and  $G_3$ .

### 4.3.3 Performance analysis and results

The BER and the received power penalty performances of the TaMZ are similar to the SMZ performances because the switched/demultiplexed signal expression at OP<sub>1</sub> of both SMZ and TaMZ are identical, (4.1) and (4.15) when  $\alpha = 0.5$  in (4.14). This section will therefore focus on the switch  $CR$  improvements and the switching stability condition depending on the balance of the TaMZ arms (i.e.  $\alpha \neq 0.5$ ). The investigations will be based on theoretical calculation as well as VPI simulation.

The TaMZ switching “on”/“off” states at the output OP<sub>*i*</sub>, (4.15) and (4.16), depend on the imbalanced/balanced states between the  $i^{\text{th}}$  and  $(i+1)^{\text{th}}$  arms, respectively. Note that for higher values of  $CR$ s in (4.10) and (4.11), the denominators, representing the non-switched signals, should be minimised as much as possible. Assuming that SOAs are identical and the couplers are perfect with factors of  $\alpha_{11} = \alpha_{12} = \alpha_{01} = \alpha_{02} = 0.5$  for C<sub>11</sub>,

$C_{12}$ ,  $C_{01}$  and  $C_{02}$ , respectively, the ideal  $CR_{OPij} \rightarrow \infty$  when the TaMZ switches input data to  $OP_i$ . However, in practice,  $\alpha_{Ij}$  or  $\alpha_{Oj}$  or both may not be equal to 0.5, therefore  $CR_{OPij}$  is reduced. This is due to the left-over power at the  $OP_j$  because of unevenly split signals at the TaMZ arms and its outputs. The inter-output  $CR$ s of the TaMZ with respect to variations of  $K_{ij}$  can be calculated from (4.10) and (4.11) by:

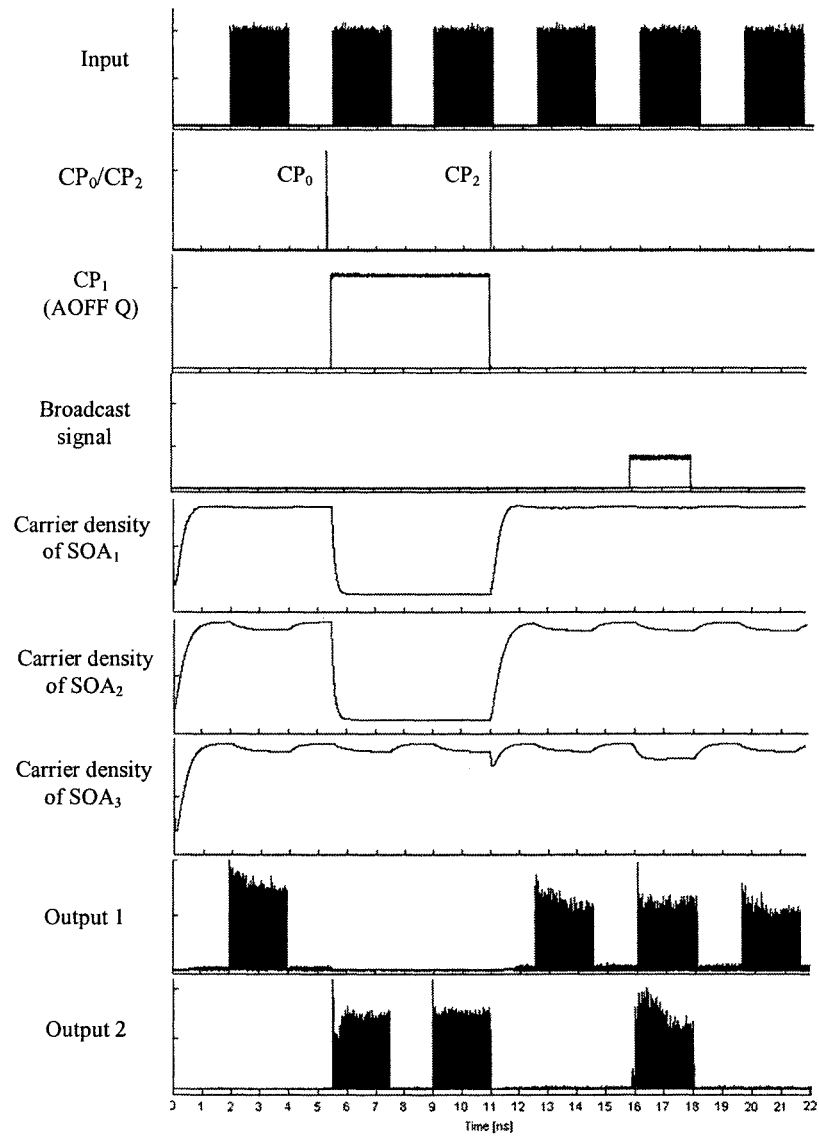
$$CR_{OP12} = \frac{G_{1-B}K_{11}^2 + K_{12}^2G_{2-I} - 2K_{11}K_{12}\sqrt{G_{1-B}G_{2-I}}\cos\Delta\phi_{1-B,2-I}}{G_{3-I}K_{21}^2 + G_{2-I}K_{22}^2 - 2K_{21}K_{22}\sqrt{G_{2-I}G_{3-I}}\cos\Delta\phi_{2-I,3-I}}, \quad (4.18)$$

$$CR_{OP21} = \frac{G_{3-I}K_{21}^2 + G_{2-CP1}K_{22}^2 - 2K_{21}K_{22}\sqrt{G_{3-I}G_{2-CP1}}\cos\Delta\phi_{3-I,2-CP1}}{G_{1-CP1}K_{11}^2 + G_{2-CP1}K_{12}^2 - 2K_{11}K_{12}\sqrt{G_{1-CP1}G_{2-CP1}}\cos\Delta\phi_{1-CP1,2-CP1}}, \quad (4.19)$$

where  $G_{i-I}$ ,  $G_{i-B}$  and  $G_{i-CP1}$  represent the initial SOA gain, SOA gains induced by the bias signal and  $CP_1$ , respectively. In the broadcasting mode (i.e. no CPs),  $CR_{OP}$  is identical for  $OP_1$  and  $OP_2$  provided that the power of the broadcast and bias signals are similar, i.e.  $G_{1-B} = G_{3-Br} \neq G_{2-I}$ , where  $G_{i-Br}$  is the gain induced by applying the broadcast signal to the SOA.

The proposed  $1 \times 2$  TaMZ switch is simulated in VPI. Figure 4.10 illustrates the operation of the TaMZ switch in both switching and broadcasting modes. Simulation parameters are given in Table 4.6, with SOA parameters given in Table 4.4. With no CPs, the 1<sup>st</sup> input packets are switched to  $OP_1$ . When an optical pulse  $CP_0$  is applied, the AOFF generates  $CP_1$  with duration  $T_{SW}$  of 5.5 ns, which is injected into  $SOA_1$  and  $SOA_2$  to switch the 2<sup>nd</sup> and 3<sup>rd</sup> input packets to  $OP_2$ . Note there is a drop in the carrier densities of  $SOA_1$  and  $SOA_2$  during  $T_{SW}$  due to  $CP_1$ . With  $CP_2$  being applied to  $SOA_3$  and  $CP_1$

exited SOA<sub>1</sub> and SOA<sub>2</sub>, the TaMZ restores itself back to a normal operation mode and switches the 4<sup>th</sup> input packet to OP<sub>1</sub>. The TaMZ broadcasts the 5<sup>th</sup> packet to OP<sub>1</sub> and OP<sub>2</sub> on the receiving the broadcast signal and returns to its normal mode in the absence of CPs, thus switching the 6<sup>th</sup> packet only to OP<sub>1</sub>.



**Figure 4.10** Pulse diagrams of input, control and output signals of TaMZ switch in switching and broadcasting operation modes

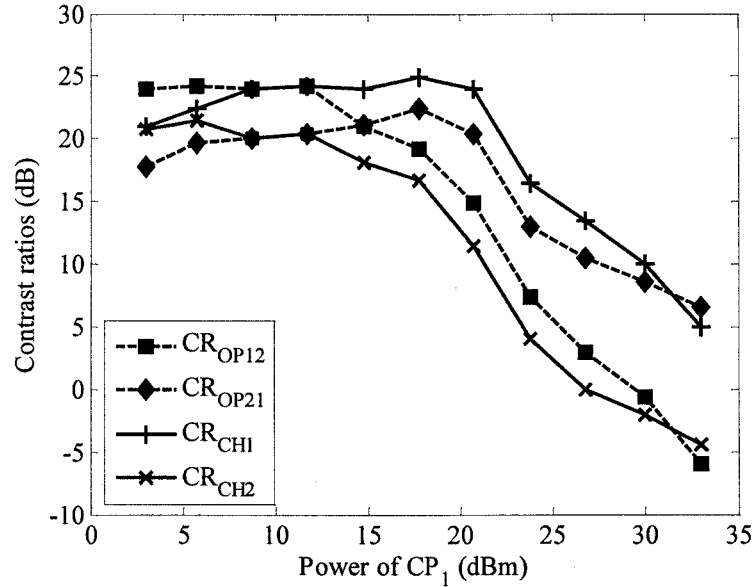


**Table 4.6** TaMZ parameters for CR and stability calculation and simulation

Parameters	Values
Input data bit rate	100 Gbit/s
Data CP <sub>0</sub> and CP <sub>2</sub> width - FWHM	2 ps
Switching window width - $T_{sw}$	5.5 ns
Packet length - $T_{pk}$	2 ns (200 bits)
Packet guard band	1.5 ns
Data pulse (peak) power	0 dBm
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Average optical continuous wave bias signal	– 3 dBm
Average broadcast signal	– 6 dBm
CP <sub>0</sub> (peak) power	33 dBm
CP <sub>1</sub> (peak) power	11.7 dBm
CP <sub>1</sub> combination factor - $\beta$	0.98
CP <sub>2</sub> (peak) power	25 dBm
$G_{1-I} = G_{2-I} = G_{3-I}$	24 dB
$G_{1-Br}$	19 dB
$G_{1-CP1} = G_{2-CP2}$	6 dB
AOFF splitting factor - $\delta$	12.5%
AOFF $P_{CW}$	0 dBm
AOFF feedback loop delay - $T_{FBL}$	0.2 ns

Also in Figure 4.10, the transient time of changing (i.e. the SOA carrier density changes) from the normal mode to switching mode is small (picoseconds), due to the ultrafast response of the SOA when interacting with the CP [155]. However, restoring back to the normal mode requires more time (hundreds of picoseconds) owing to the SOA carrier relaxation time inherited from the SOA-based switches. A packet guard band should therefore be employed to ensure full gain recovery of the switch.

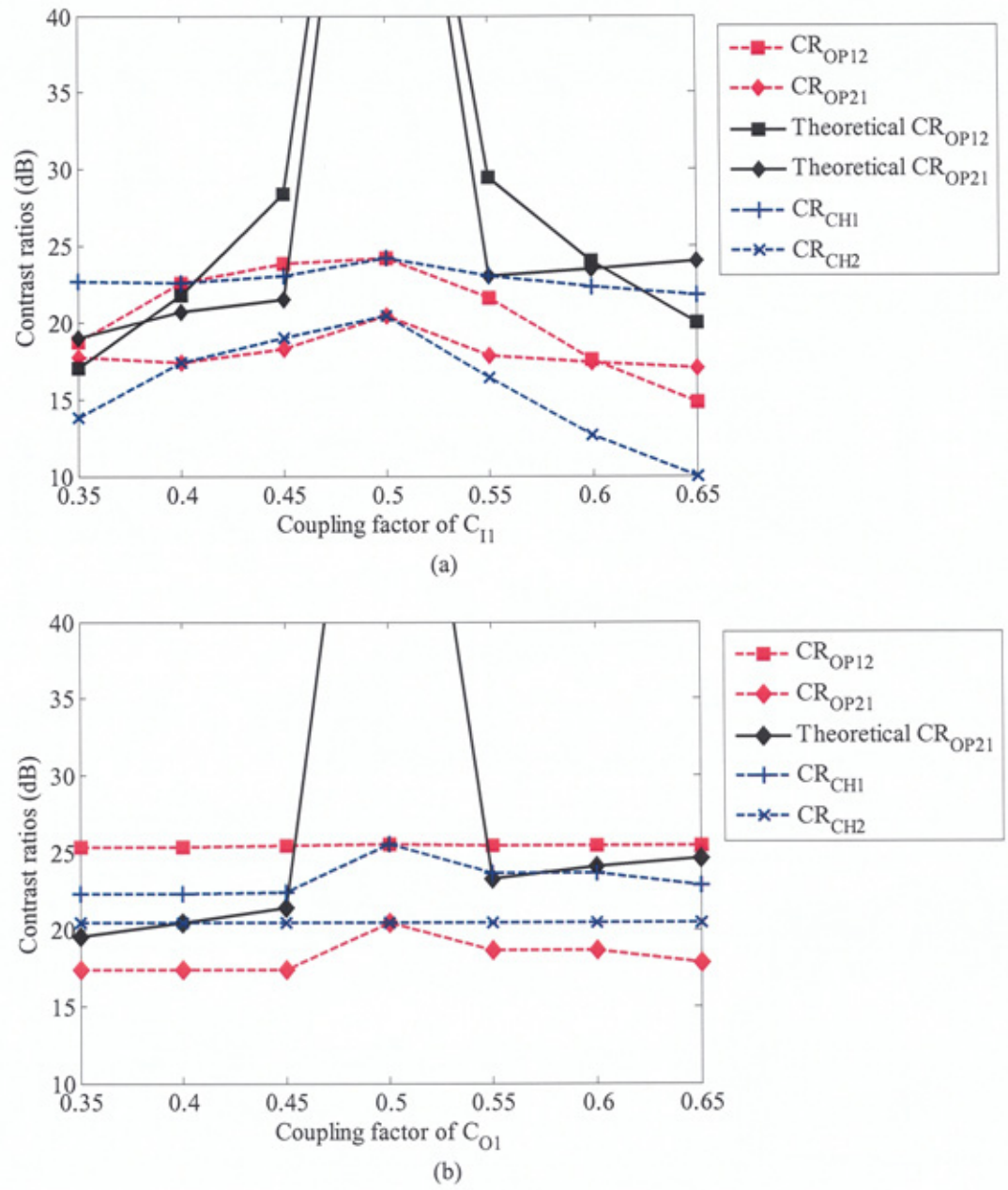
Figure 4.11 displays the simulation results of  $CR$ s against the  $CP_1$  power for  $CR_{OPij}$  and  $CR_{CHi}$ . The  $CR$ s values are relatively high and constant at  $\sim 20$  dB over a wide power range of  $CP_1$  (0-20 dBm) showing a considerable improvement when compared with the SMZ, see Figure 4.8. For both  $CR_{OPij}$  and  $CR_{CH2}$ , the improvement is  $> 10$  dB. For  $CR_{CH1}$ , the value is almost the same as the SMZ; however, TaMZ offers a larger range of  $CP_1$  power in comparison to the SMZ switch. For higher values of  $CP_1$  power,  $CR$ s drop due to a deeper SOA gain saturation requires a longer recovery time ( $> 1.5$  ns), thus resulting in a higher residual power of non-switched signals. Note  $CR_{OP12}$  and  $CR_{CH1}$  decrease at a faster rate than their counterparts  $CR_{OP21}$  and  $CR_{CH2}$ . This is because a higher  $CP_1$  power will further reduce the gain levels of  $SOA_1$  and  $SOA_2$  ( $G_{1-CP1}$  and  $G_{2-CP1}$ ) during  $T_{SW}$ , thus increasing  $SW_2$  gain (4.16) in comparison to a fixed  $SW_1$  gain induced by a constant-power bias signal when no  $CP_1$  is applied.



**Figure 4.11** The simulated contrast ratios against the power of  $CP_1$

The investigation of the  $CR_{OP}$  performance against the variations of the coupling factors of  $C_{I1}$  and  $C_{O1}$  ( $\alpha_{I1}$  and  $\alpha_{O1}$ , respectively), which affect the stability (balance) of the upper interferometer, is depicted in Figure 4.12(a). Both predicted and simulated results show  $CR$ s changes when  $\alpha_{I1} \neq 0.5$ .  $CR_{OP21}$  display much smaller changes in comparison to the  $CR_{OP12}$ . This is due to the power difference between the two arms of the lower interferometer being less than that difference in the upper interferometer. In contrast, in Figure 4.12(b) the  $CR$ s change very little with the  $C_{O1}$  variation compared with the  $C_{I1}$ . This could be explained by the factor  $K_{ij}$  in (4.14), where  $\alpha_{I1}$  are the contributors for  $K_{11}$ ,  $K_{12}$  and  $K_{22}$  whereas  $\alpha_{O1}$  only affects  $K_{21}$ . The predicted results for  $CR_{OPij}$  at  $\alpha_{I1} = 0.5$  and  $CR_{OP12}$  are not shown in Figure 4.12(a) and (b), respectively, since they reach infinity in correspondence with (4.18) and (4.19). Note the predicted values of  $CR_{OP}$  depart from simulated data. This is due to the simulation model accounting for (i) the cross gain modulation (XGM) effect between CPs and input data which results in a small reproduced power emerging at OPs and (ii) the ripples of  $SOA_{1\&2\&3}$  gains cause the left-over power at OPs when switched-off, whereas in the theoretical calculation, XGM is neglected and the gains are assumed equal (see Table 4.6)

In conclusion, the proposed TaMZ maintains the key features of the SMZ and but offers improved  $CR$ s, a broadcast capability and signal blocking by means of controlling the CPs.



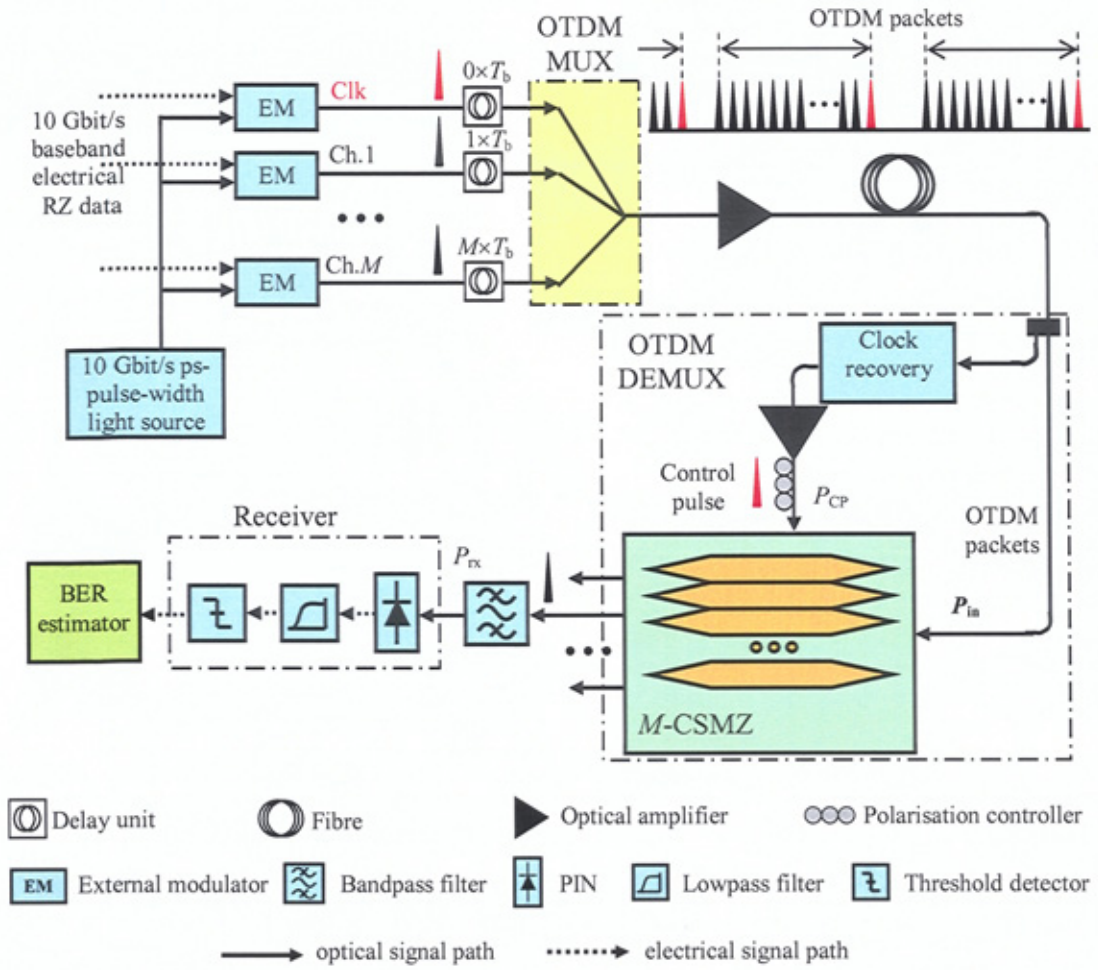
**Figure 4.12** Contrast ratios against the coupling factor values: (a)  $C_{11}$  and (b)  $C_{01}$  for a range of 0.35 - 0.65

#### **4.4 $1 \times M$ Chained Symmetric Mach-Zehnder OTDM Demultiplexer**

The OTDM demultiplexer, or optical add/drop multiplexer (OADM) for extracting a single data channel, is relatively straightforward using a single UF-OSW. However, simultaneously demultiplexing multi-channels is a challenging task requiring complex implementation such as a photonic serial-to-parallel converter (PSPC) based on the Lithium Niobate electro-opto modulator [200], surface-emitted second-harmonic generation (SESHG) employing hybridised semiconductor/silica waveguide circuits [201], and an array of optical single-channel SOA-based UF-OSW demultiplexers [7, 152, 202]. Among these structures, the latter is the most promising approach owing to its extremely narrow demultiplexing window (i.e. switching window) in the order of picoseconds or sub-picosecond, which is suitable for the existing and future ultrahigh-capacity OTDM systems. Nevertheless, multiple channel demultiplexing, based on an array of SMZs, is relatively complex due to the utilisation of a large number of SOAs (required  $2 \times M$  SOAs for  $M$ -channel demultiplexing). In this thesis, work on a novel multiple-channel OTDM demultiplexer, based on a chained SMZ configuration, is proposed which uses a reduced number of SOAs (to  $M+1$ ) in comparison to an array of individual SMZs.

##### **4.4.1 CSMZ operation principle**

An asynchronous OTDM system, as shown in Figure 4.13, includes a multiple-channel demultiplexer and other modules as described in Section 3.3.3.



**Figure 4.13** A schematic diagram of asynchronous OTDM system using  $M$ -CSMZ

The CSMZ architecture is presented in Figure 4.14 comprising an  $1 \times M$  input splitter,  $M$  of 3-dB  $2 \times 2$  input  $C_{I,x}$  and output  $C_{O,x}$  couplers ( $x$  is the channel number),  $2 \times 1$  combiners,  $1 \times 2$  splitters (see Table 4.5) and identical SOAs in  $M+1$  CSMZ arms ( $A_1$  to  $A_{M+1}$ ). The inclusion of 3-dB attenuators located at each arm will ensure identical optical powers at the SOAs and  $C_{O,x}$  couplers, thereby ensuring a balanced state between each pair of adjacent arms. Thus, in the absence of a CP, no input signal emerges at the CSMZ output ports.



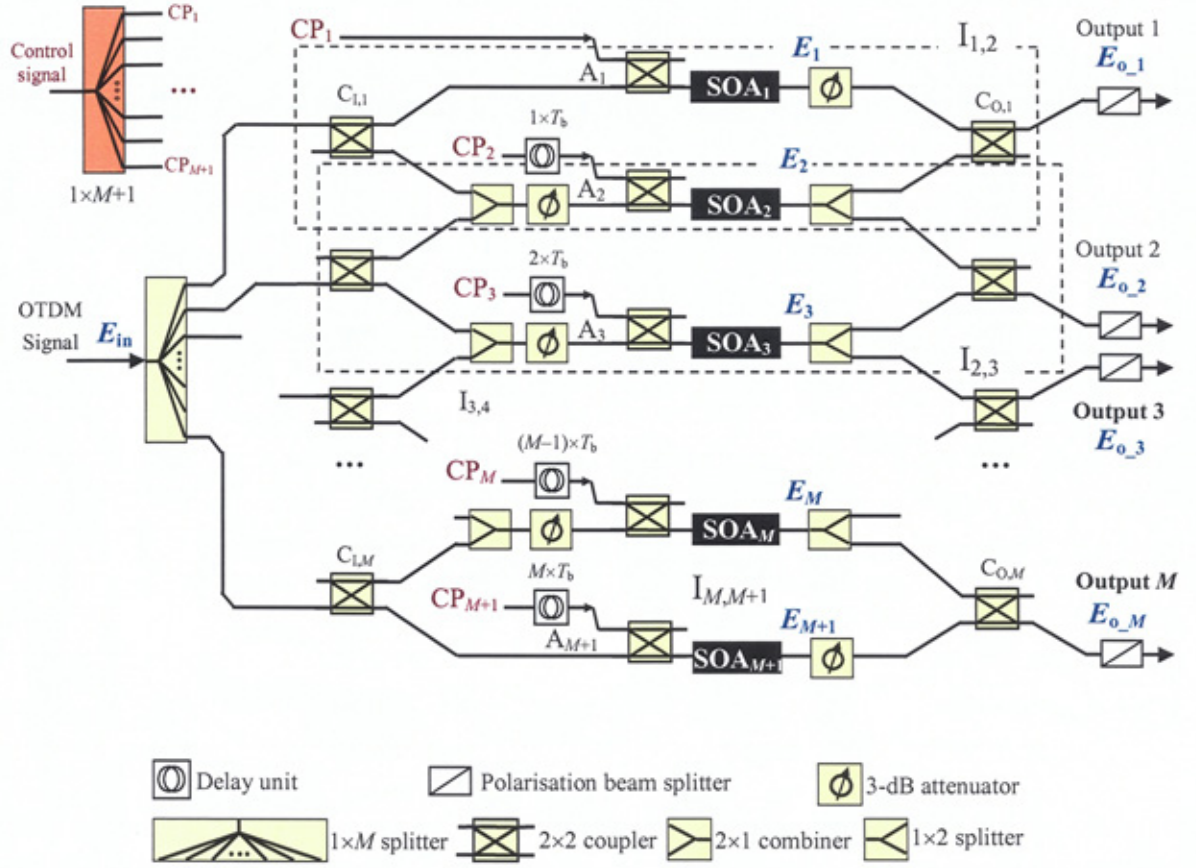


Figure 4.14 Circuit diagram of  $M$ -CSMZ demultiplexer

For demultiplexing purposes, the extracted clock signal is split into  $M+1$  high-powered CPs with equal intensities.  $CP_1$  is applied to  $SOA_1$ , just prior to the arrival of the data on channel 1 to the interferometer  $I_{1,2}$ , to set  $I_{1,2}$  to an imbalanced state (i.e.  $SOA_1$  and  $SOA_2$  having different gain and phase profiles), thus demultiplexing the data on channel 1 to output 1. Since all other interferometers  $I_{k,k+1}$  ( $1 < k \leq M$ ) are still in the balanced state, there should be no signal emerging from the other outputs.  $CP_2$  (delayed by  $T_b$ ) applied to  $SOA_2$  results in two simultaneous effects: (i) restoration of a balanced state in  $I_{1,2}$  and (ii) the creation of an imbalanced state in  $I_{2,3}$  because of the gain and phase

difference between SOA<sub>2</sub> and SOA<sub>3</sub>. Thus, the CSMZ demultiplexes the data on channel 2 to the CSMZ output 2. Similarly, by applying the delayed CPs (delayed by  $(x-1) \times T_b$ ) to the relevant SOA<sub>s<sub>x</sub></sub> the corresponding  $x^{\text{th}}$  channel could be demultiplexed. To complete the demultiplexing of the  $M^{\text{th}}$  channel, CP <sub>$M+1$</sub>  is applied to A <sub>$M+1$</sub>  in order to restore the balanced state in I <sub>$M,M+1$</sub> .

Assuming that the electrical field of the input signal is  $E_{\text{in}}$  [28], the fields at the CSMZ output ports are determined by:

$$\begin{aligned}
 E_{o\_1} &= 0.5E_{\text{in}}M^{-0.5} \left[ K_{1,1}a_1e^{-j\phi_1} - K_{1,2}a_2e^{-j\phi_2} \right] \\
 E_{o\_m} &= 0.5E_{\text{in}}M^{-0.5} \left[ K_{m,1}a_{m+1}e^{-j\phi_{m+1}} - K_{m,2}a_me^{-j\phi_m} \right] \\
 E_{o\_m+1} &= 0.5E_{\text{in}}M^{-0.5} \left[ K_{m+1,1}a_{m+1}e^{-j\phi_{m+1}} - K_{m+1,2}a_{m+2}e^{-j\phi_{m+2}} \right] , \\
 E_{o\_M} &= 0.5E_{\text{in}}M^{-0.5} \left[ K_{M,1}a_{M+1}e^{-j\phi_{M+1}} - K_{M,2}a_Me^{-j\phi_M} \right]
 \end{aligned} \tag{4.20}$$

where  $a_k$  and phase  $\phi_k$  are defined in Section 4.3 ( $1 \leq k \leq M+1$ ).  $M$  is even and the coefficients  $K_{ij}$  are computed by (4.21) where  $\alpha_{I,x}$  and  $\alpha_{O,x}$  are the coupling factors of the C<sub>I,x</sub> and C<sub>O,x</sub> couplers, respectively:



$$\begin{aligned}
K_{1,1} &= (1 - \alpha_{1,1})^{1/2} (1 - \alpha_{0,1})^{1/2}; \quad K_{1,2} = \frac{1}{2} (\alpha_{1,1}^{1/2} + \alpha_{1,2}^{1/2}) \alpha_{0,1}^{1/2} \\
K_{m,1} &= \frac{1}{2} (1 - \alpha_{0,m})^{1/2} [(1 - \alpha_{1,m})^{1/2} + (1 - \alpha_{1,m+1})^{1/2}]; \quad K_{m,2} = \frac{1}{2} \alpha_{0,m}^{1/2} (\alpha_{1,m-1}^{1/2} + \alpha_{1,m}^{1/2}) \\
K_{m+1,1} &= \frac{1}{2} (1 - \alpha_{0,m+1})^{1/2} [(1 - \alpha_{1,m})^{1/2} + (1 - \alpha_{1,m+1})^{1/2}]; \quad K_{m+1,2} = \frac{1}{2} \alpha_{0,m+1}^{1/2} (\alpha_{1,m+1}^{1/2} + \alpha_{1,m+2}^{1/2}) \\
K_{M,1} &= (1 - \alpha_{1,M})^{1/2} (1 - \alpha_{0,M})^{1/2}; \quad K_{M,2} = \frac{1}{2} \alpha_{0,M}^{1/2} (\alpha_{1,M-1}^{1/2} + \alpha_{1,M}^{1/2})
\end{aligned} \tag{4.21}$$

The demultiplexing SW gains can therefore be expressed from (4.20) with  $SW_x = P_{o\_x} / P_{in} = (E_{o\_x} E_{o\_x}^*) / (E_{in} E_{in}^*)$  by the followed:

$$\begin{aligned}
SW_1 &= \frac{1}{4M} [K_{1,1}^2 G_1 + K_{1,2}^2 G_2 - 2K_{1,1} K_{1,2} \sqrt{G_1 G_2} \cos \Delta\phi_{1,2}] \\
SW_{m+1} &= \frac{1}{4M} [K_{m+1,1}^2 G_{m+1} + K_{m+1,2}^2 G_{m+2} - 2K_{m+1,1} K_{m+1,2} \sqrt{G_{m+1} G_{m+2}} \cos \Delta\phi_{m+1,m+2}] \\
SW_m &= \frac{1}{4M} [K_{m,1}^2 G_{m+1} + K_{m,2}^2 G_m - 2K_{m,1} K_{m,2} \sqrt{G_m G_{m+1}} \cos \Delta\phi_{m,m+1}] \\
SW_M &= \frac{1}{4M} [K_{M,1}^2 G_{M+1} + K_{M,2}^2 G_M - 2K_{M,1} K_{M,2} \sqrt{G_M G_{M+1}} \cos \Delta\phi_{M,M+1}]
\end{aligned} \tag{4.22}$$

#### 4.4.2 Performance analysis

Similar to the TaMZ, the CSMZ and SMZ have similar noise characteristics due to their identical SWs, as in (4.1) and (4.22). However, the BER and  $\Delta P_{rx}$  of different demultiplexed channels are greatly dependent on the balanced states of the CSMZ arms,

which will be addressed in this section. For the demultiplexed  $x^{\text{th}}$  data channel, the BER is estimated by:

$$\text{BER}_{x,u/d} = 0.5 \operatorname{erfc}(Q_{x,u/d} / \sqrt{2}), \quad (4.23)$$

where the  $Q$  factor from (3.15) is expressed by the eye closure (EC):

$$Q_{x,u/d} = \text{EC}_{x,u/d} / (\sigma_{x,0} + \sigma_{x,1}). \quad (4.24)$$

EC is illustrated in the eye diagram depicted in Figure 4.15 at  $t_{\text{sampling}}$  [124] and determined as:

$$\text{EC}_{x,u/d} = K P_{\text{in}} [\text{SW}_{x,1}(\alpha_{I/O,u/d}) - \text{SW}_{x,0}(\alpha_{I/O,u/d})], \quad (4.25)$$

where  $P_{\text{in}}$  is an average CSMZ average input power (Figure 4.13) and  $K$  is a factor proportional to the photodiode detector responsivity, filter loss and coupling efficiencies given in Section 3.3.2. The subscript 0 or 1 in  $\text{SW}_x$  denotes the OFF/ON states of the CSMZ  $x^{\text{th}}$  output.  $\sigma_{x,0/1}$  is the standard deviation of the total noise power for bit 0 or 1 (0/1) given in Section 3.3.2 and u and d represent the undistorted and distorted EC for  $\alpha = 0.5$  (ideal) and  $\alpha \neq 0.5$ , respectively. Assuming that the ASE noise of SOA is random, coupling ratio variations will have no effect on the summed ASE power at each CSMZ output. From (4.21) - (4.25), it is shown that the BER performance will depend on the input/output coupling ratios, which are evaluated in the next section.

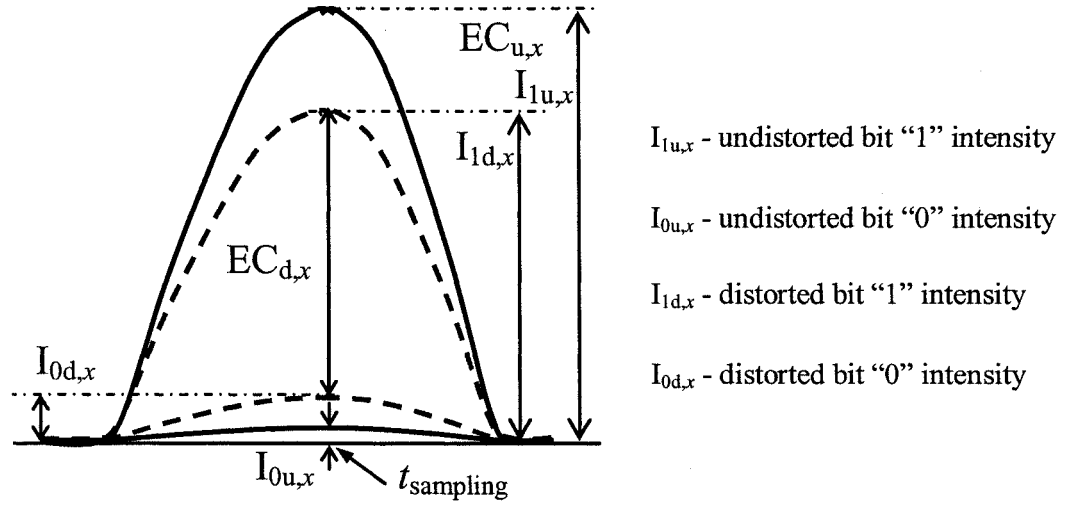


Figure 4.15 Eye diagram of the  $x^{\text{th}}$  channel [124]

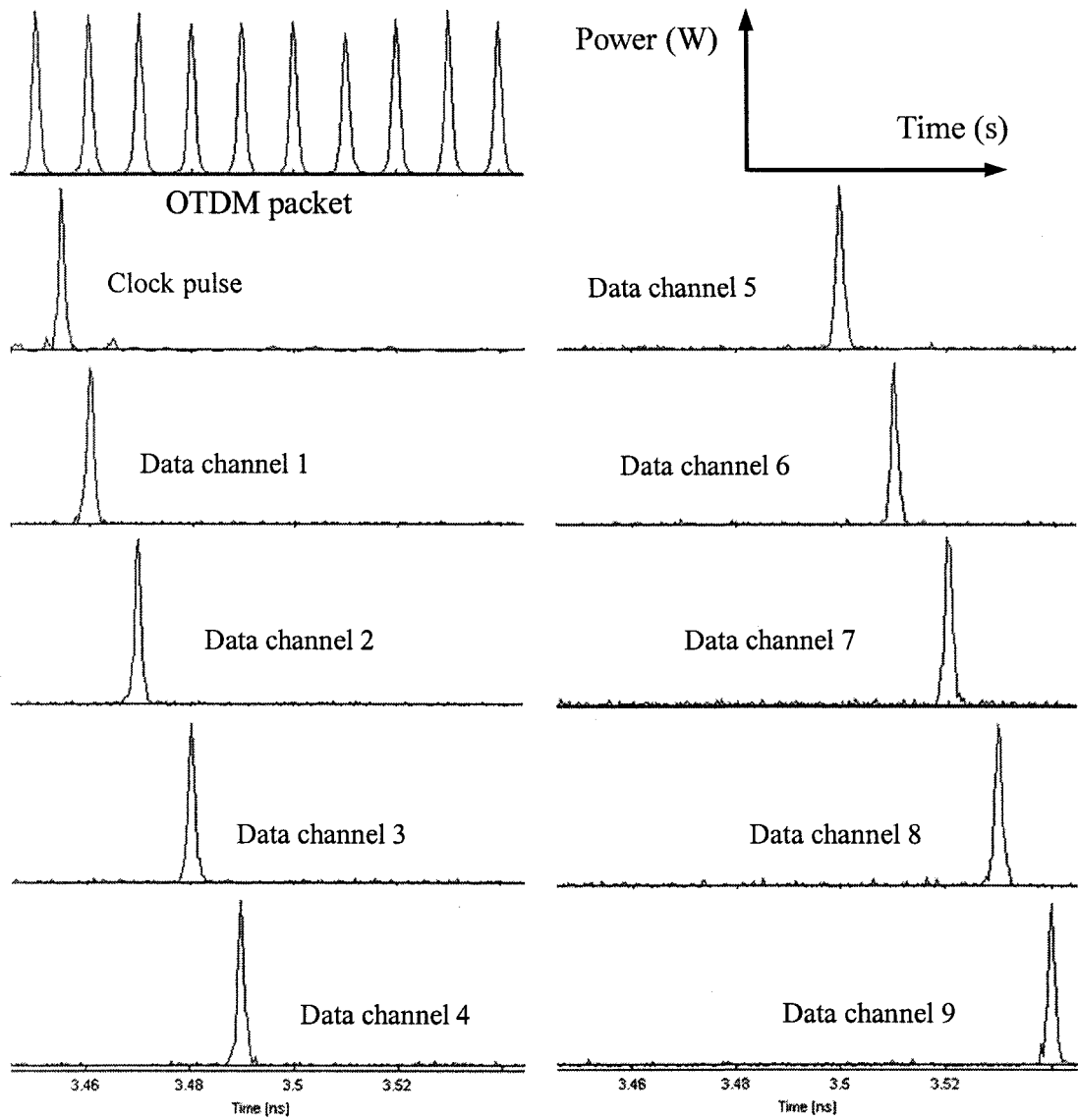
#### 4.4.3 Performance results and discussions

CSMZ is adopted for a parallel 100-to-10 Gbit/s demultiplexer and investigated in theory and simulation. OTDM packets are generated from nine 10-Gbit/s sources with a PRBS of  $2^{15} - 1$  with an additional clock signal channel for synchronisation purpose. A guard-slot of 0.5 ns is used between consecutive packets to ensure gain recovery in the clock recovery unit as required. CSMZ parameters for calculation and simulation are given in Table 4.7 and SOA parameters were presented in Table 4.2.

**Table 4.7** CSMZ parameters for OTDM demultiplexing, BER calculation and simulation

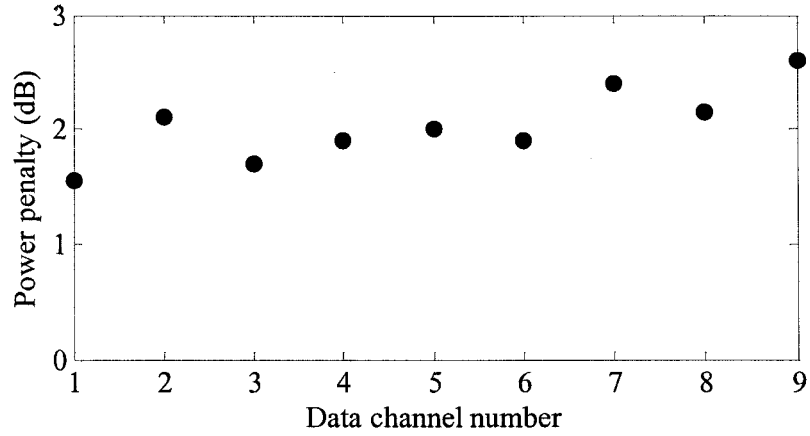
Parameters	Values
OTDM aggregate bit rates	100 Gbit/s
Baseline bit rate	10 Gbit/s
Number of data channels	9
PRBS sequence	$2^{15} - 1$
Data and CP width - FWHM	2 ps
Switching window width - $T_{sw}$	10 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Data pulse (peak) power	1.75 dBm (1.5 mW)
CP (peak) power	10 dBm (10 mW)
Packet guard band	0.5 ns
Optical filter loss - $L_f$	- 2 dB
Optical bandwidth - $B_o$	300 GHz
Electrical bandwidth - $B_e$	$0.7 \times 10$ GHz
Load resistance - $R_L$	50 $\Omega$
Photodetector responsivity - $R_p$	1 A/W
Power spectral density - $i_a^2$	10 pA/Hz <sup>1/2</sup>
RIN variance of TOAD - $RMS_{RIN-TOAD}$	0.5 ps
RIN of transmitter - $RIN_T$	- 20 dB

Figure 4.16 illustrates the time waveforms of the demultiplexed data channels by 9-channel CSMZ and the extracted clock pulse. The clock signal is separately extracted using a clock extraction unit, which will be discussed in Chapter 6.



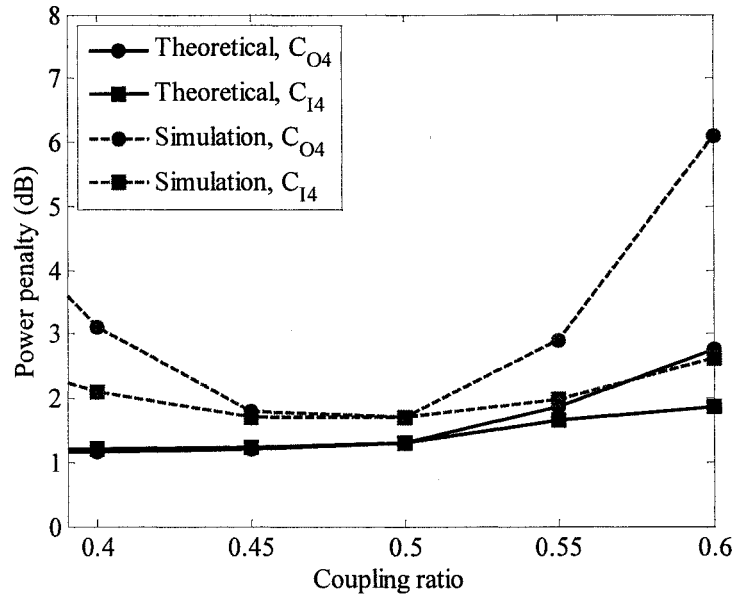
**Figure 4.16** Simulated time waveforms of 100-to-10 Gbit/s OTDM demultiplexed data channels and extracted clock pulse

Depicted in Figure 4.17 are the power penalties for a range of demultiplexed data channels, showing an average value of  $\sim 2$  dB (1.5 to 2.5 dB) provided that all coupling factors are set at 0.5.

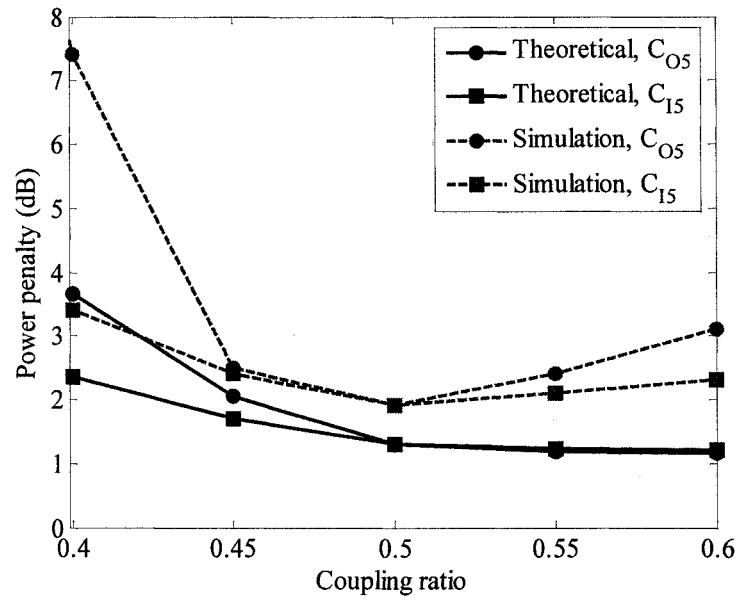


**Figure 4.17** Power penalties for different demultiplexed channels

However, the power penalties change with the CSMZ coupling ratios  $\alpha$  as outlined in Figure 4.18(a) and (b) for even and odd channels, respectively. The power penalties (predicted and simulated) increase by a few dB for  $\alpha_O \neq 0.5$  and by 1 dB for  $\alpha_I \neq 0.5$ . This can be explained from (4.21) where the dominant term is  $\alpha_{O,x}$  (similar to TaMZ) and consequently SW, EC and hence, the power penalty becomes more sensitive to  $\alpha_{O,x}$  than to  $\alpha_{I,x}$ .



(a)



(b)

**Figure 4.18** Predicted and simulate power penalties against the CSMZ coupling ratio  $\alpha$  for (a) even (4<sup>th</sup>) and (b) odd (5<sup>th</sup>) channels

The power penalties incurred also depend on which data channel is demultiplexed. For even channels, the power penalty is lower for  $\alpha_{I/O,x} < 0.5$  in comparison to  $\alpha_{I/O,x} > 0.5$ , whereas the opposite is true for odd channels, see Figure 4.18(a) and (b), respectively. The reason for this is as follows. When demultiplexing the  $x^{\text{th}}$  channel, the SOAs are sequentially excited by  $\text{CP}_x$  and  $\text{CP}_{x+1}$ , thereby the data signal in the lower arm  $A_{x+1}$  experiences more amplification gain than that in the upper arm  $A_x$ , because  $G_{x+1-\text{SOA}_{x+1}} > G_{x-\text{SOA}_x}$ , see Figure 4.14(b). For odd channels, the demultiplexed signal intensity  $I_{1d,x}$  (Figure 4.15) is greater for  $\alpha_{I/O,x} > 0.5$  in comparison to  $\alpha_{I/O,x} < 0.5$  (due to the greater contribution of signal from the lower arm). As a result  $\text{EC}_{x,d}(\alpha_{I/O,x} > 0.5) > \text{EC}_{x,d}(\alpha_{I/O,x} < 0.5)$ , thus contributing to a lower BER and power penalty. However, for even channels,  $\text{EC}_{x,d}(\alpha_{I/O,x} > 0.5) < \text{EC}_{x,d}(\alpha_{I/O,x} < 0.5)$ , thus resulting in a higher power penalty for  $\alpha_{I/O,x} > 0.5$  compared to  $\alpha_{I/O,x} < 0.5$ .

## 4.5 Summary

In this chapter, the ultrafast SMZ optical switch was studied and a new unequal CPs scheme was proposed to further improve its *RCXT* performance. It was shown that the power penalty for a SMZ with unequal CPs has been improved (i.e. reduced) by  $\sim 1$  dB in comparison to that achieved with equal CPs scheme. The chapter continued with an investigation of inter-channel and inter-output *CR* for a SMZ switch, which was found to be relatively low ( $< 15$  dB). The TaMZ was introduced and analysed to address this low *CR* using two high *CR* output-1s of two common-arm SMZs as its new outputs. The TaMZ not only offered an improved *CR* performance ( $\sim 20$  dB), but also provided the



broadcast and blocking signal capabilities in comparison to the SMZ. In addition, this chapter extended the TaMZ structure to construct a new  $1 \times M$  CSMZ switch which offered a reduced complexity for a multiple-channel OTDM demultiplexer. The effects of coupling ratios on the TaMZ and CSMZ operation stabilities and power penalties have been studied.

In order to achieve a flat gain response in a MZ based device, a controlling scheme based on an AOFF was proposed which will be characterised in Chapter 6.

The performance results for the SMZ with unequal CPs can be found in papers [A13] and [A14] and the findings for the TaMZ were published in paper [A10]. For CSMZ the analysis and results can be found in publication [A17] and in the paper under-review [A25].

On the basis of understanding the properties of ultrafast optical switches and their characteristics, in the following chapters, the MZ-based switches will be employed as the building blocks in the design of the proposed PPM-HP router.

## **CHAPTER 5**

# **ROUTER WITH A PULSE-POSITION-MODULATION BASED PACKET HEADER PROCESSING UNIT**

### **5.1 Introduction**

The next generation optical network will rely on all-optical header processing and switching technologies to provide transparent optical paths for packet routing to ensure a high speed and high throughput data transmission. A number of the existing all-optical header processing and switching schemes were highlighted in Chapters 1 and 2 based on two main routing approaches: (i) pre-defined routing path information embedded within a packet header and (ii) correlation of the packet header address with look-up routing table entries. Both approaches offer continuous optical routing paths, however at the cost of a low packet payload efficiency (due to a longer packet header) and complex all-optical correlation circuits (due to a large look-up routing table).

This chapter proposes an alternative structure for the packet header and the routing table based on the pulse-position-modulation (PPM) format to achieve all-optical routing, offering reduced header processing time and complexity. The chapter begins with an

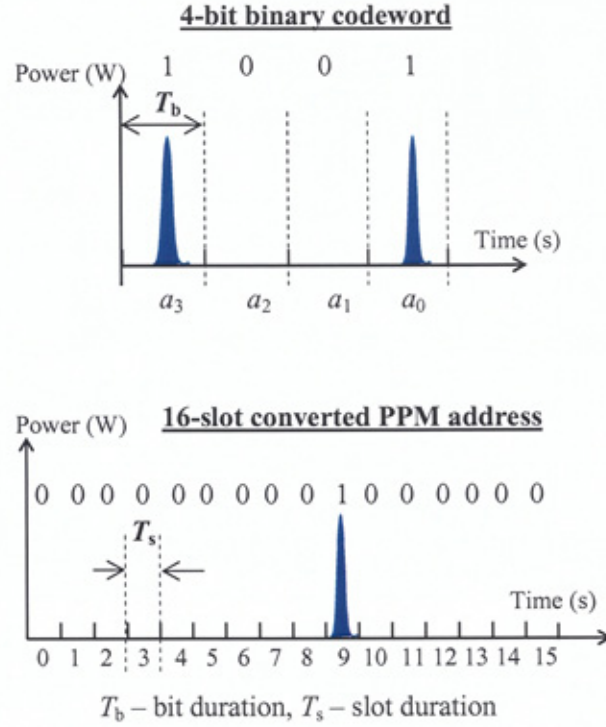
introduction to the PPM concept and the principle of a new pulse-position routing table (PPRT). On the basis of this, routers with a PPM based packet header processing (PPM-HP) scheme are developed for single and multiple-wavelength packet switching systems. In addition, all elements of the proposed router are systematically outlined. The chapter will conclude with final remarks on the PPM-HP router.

## 5.2 Pulse Position Modulation

In the optical transparent core network given in Figure 2.2, the data header of a  $N$ -bit binary codeword contains the destination address, see Figure 2.5, where each bit “1” is encoded as an optical pulse. In PPM a  $N$ -bit binary codeword is mapped into a single frame of  $2^N$ -slot length with a short pulse located at the  $m_A^{\text{th}}$  slot, the position of which corresponds to the decimal value of the  $N$ -bit binary packet header address. A  $N$ -bit address of  $[a_{N-1} a_{N-2} \dots a_2 a_1 a_0]$  will have the decimal metric  $m_A$  is computed by:

$$m_A = a_{N-1} \times 2^{N-1} + a_{N-2} \times 2^{N-2} + \dots + a_2 \times 2^2 + a_1 \times 2^1 + a_0 \times 2^0. \quad (5.1)$$

Thus, in PPM the information is conveyed by the position ( $m_A$ ) of a single pulse within a fixed frame [203]. Figure 5.1 illustrates an example of a 4-bit codeword “1001”, i.e.  $m_A = 9$ , thus the single optical pulse is located at the 9<sup>th</sup> slot. In Figure 5.1,  $T_b$  and  $T_s$  are the bit duration and slot duration, respectively.



**Figure 5.1** Example of a 4-bit binary (address) codeword and the equivalent 16-slot PPM frame (the PPM address)

### 5.3 Pulse Position Routing Table

A router typically consists of a conventional  $2^N$ -entry look-up routing table which defines an output port (out of  $M$  possible router outputs) for a packet with a specific  $N$ -bit address, i.e. routing information, see Figure 2.6. A router makes a routing decision by correlating and matching the packet header address with a unique entry in the routing table. In the worst case, i.e. where all possible entries are checked (exhaustive correlation), the router needs to perform  $2^N$   $N$ -bitwise correlations. When the number of routing table entries is large (order of hundreds), the correlation process requires either (i) a lengthy sequential correlation using a minimum number of optical logic gates (or optical correlators) or (ii) extensive use of a large number of parallel optical correlators

for parallel correlations. In both cases, it requires a compromise between the header recognition speed and the router's complexity/costs. Therefore, it is advantageous to reduce the number of routing table entries while fully preserving the routing information to make the header recognition scheme robust.

In a conventional routing table the number of its entries is the number of possible  $2^N$  address patterns, with each entry dedicated to an output port, and the processing time is long for large scale routing tables (i.e.  $2^N$  entries). The pulse-position routing table (PPRT) is an alternative scheme for creating a routing table with reduced size by limiting the number of entries to the number of router output ports  $M$ , and therefore shortening the processing time. A PPRT is constructed as follows:

- 1) From the conventional routing table, all decimal metrics of address patterns ( $P$ ) having the same router output  $\#m$  are grouped into a set  $\mathbf{P}_m$ . The number of  $\mathbf{P}_m$  elements is  $N_m = \text{length}(\mathbf{P}_m)$
- 2) The  $m^{\text{th}}$  entry in the PPRT is a  $2^N$ -slot PPM frame which accommodates  $N_m$  optical pulses. These pulses are located at the positions corresponding to the decimal metrics given in  $\mathbf{P}_m$ .

Table 5.1 represents a PPRT generation for  $M = 3$  outputs based on the conventional routing table which was given in Figure 2.6 with  $N = 4$  bits. Each generated PPRT entry in the table is a 16-slot PPM frame with a number of pulses positioned at dedicated slots corresponding to the decimal weights of the address patterns assigned to a particular

node output. When a packet header address matches with entries having decimal metrics of 0, 2, 6, 9, 10, 12 and 14, the whole packet will be forwarded to the router output port 1. For the set  $P_1 = [0, 2, 6, 9, 10, 12 \text{ and } 14]$  in the PPRT, the entry 1 has short duration pulses located at the positions 0, 2, 6, 9, 10, 12 and 14. Similarly for the sets  $P_2$  and  $P_3$  the PPRT entries 2 and 3 will have pulses at positions 1, 3, 4, 8, 13, 14 and 1, 5, 7, 10, 11, 14, 15, respectively.

**Table 5.1** 3-entry PPRT generated from the conventional look-up routing table in Figure 2.6

Sets (P)	Address patterns	Decimal metrics in the set	PPRT entries
$P_1$	0 0 0 0 0 0 1 0 0 1 1 0 1 0 0 1 1 0 1 0 1 1 0 0 1 1 1 0	{0,2,6,9,10,12,14}	
$P_2$	0 0 0 1 0 0 1 1 0 1 0 0 1 0 0 0 1 1 0 1 1 1 1 0	{1,3,4,8,13,14}	
$P_3$	0 0 0 1 0 1 0 1 0 1 1 1 1 0 1 0 1 0 1 1 1 1 1 0 1 1 1 1	{1,5,7,10,11,14,15}	

Packet (PK)

Assuming that a packet header address with a decimal metric of 6 is converted to the PPM format, the PPM address has a pulse located in the 6<sup>th</sup> slot (see Table 5.1). Correlation (using a single-bitwise Boolean AND operation) of the PPM address with

the PPRT entries will result in an output only for the PPRT entry with a pulse at the 6<sup>th</sup> position. In unicast transmission mode, only a single pulse is located amongst the identically indexed slots of all entries, whereas in multicast and broadcast transmission modes, identically indexed slots of entries can have many pulses. For example, in the case a pulse appears at all entries (i.e. at the 1<sup>st</sup> or the 10<sup>th</sup> slot), when the incoming packet header address pattern is either “0001” or “1010”, the packet is broadcasted to all outputs. However, when there is no pulse located at all identically indexed slots in the PPRT, there is no packet being switched out, i.e. the packet is dropped (deleted).

## 5.4 Packet Switching Router based on PPM-HP

In this section, the design of the PPM-HP router architectures for both single and multiple wavelengths will be presented to realise the proposed PPM address conversion and PPRT concepts.

### 5.4.1 Single wavelength PPM-HP router

The diagram of the proposed single wavelength  $1 \times M$  PPM-HP router is depicted in Figure 5.2. The PPM-HP router is composed of a number of main modules including the clock extraction module (CEM), pulse-position-modulation header extraction module (PPM-HEM), pulse position routing table (PPRT), AND gates, optical switch controller (OSWC) and an optical switch (OSW) module. The incoming packet  $PK(t)$  is split and applied to the CEM, PPM-HEM and OSW with the delays of 0,  $T_{CEM}$  (required time for clock extraction) and  $T_{PPM-HP}$  (total required time for PPM header processing),





...,  $T_{N-1}$  to ensure that all  $a_i$  are simultaneously applied to the control inputs of the switches in PPM-ACM before being applied to the control inputs of  $N$   $1 \times 2$  switches for PPM address conversion in PPM-ACM. The input to the PPM-ACM is  $CP_{\text{PPM-ACM}}(t)$ , where  $CP_{\text{PPM-ACM}}(t) = \kappa \text{CLK}(t + T_{\text{ACM}})$ . Based on the values 0/1 of address bits  $a_i$  ( $i = 0, 1, \dots, N-1$ ),  $CP_{\text{PPM-ACM}}(t)$  propagates through  $N$  switches, accumulating a total delay of  $m_A \times T_s$ .

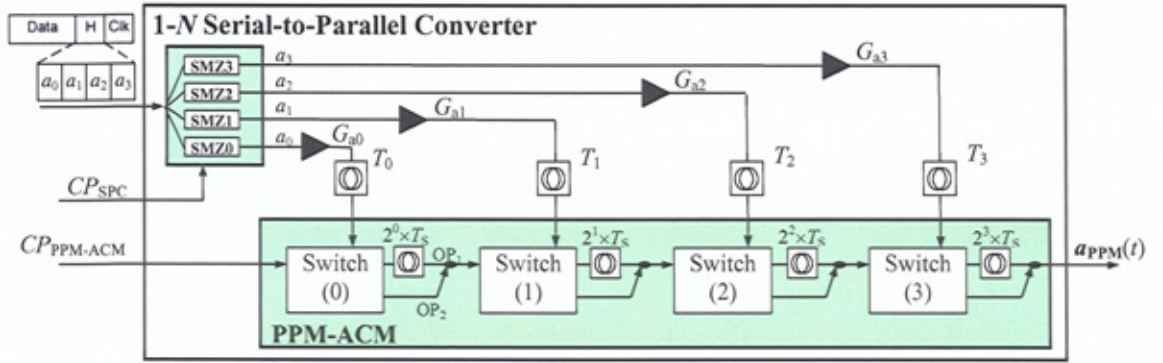


Figure 5.3 All-optical PPM header extraction module

The output of the PPM-HEM converted into a PPM-address in the output  $a_{\text{PPM}}$  is given by:

$$a_{\text{PPM}}(t) = CP_{\text{PPM-ACM}} \left( t + \sum_{i=0}^{N-1} a_i \times 2^i \times T_s \right), \quad a_i \in \{0,1\}. \quad (5.2)$$

Note that the additional delay induced to  $CP_{\text{PPM-ACM}}(t)$  is equal to the product of the decimal value of the header address and a PPM slot duration  $T_s$ . The delay is generated using a series of  $1 \times 2$  optical switches with high on/off extinction ratio based on a SMZ employing a SOA (details in Chapter 6). At the  $n^{\text{th}}$  switch ( $n = 0, 1, \dots, N-1$ ), a single

input pulse  $CP_{\text{PPM-ACM}}\left(t + \sum_{i=0}^{n-1} a_i \times 2^i \times T_s\right)$  is either switched to the output 1 (OP<sub>1</sub>) or output 2 (OP<sub>2</sub>) depending on the status “1” or “0” of the address bit  $a_i$ , respectively. The switched pulse at OP<sub>1</sub> will experience a delay of  $2^i \times T_s$  whereas there will be no delays at OP<sub>2</sub>. In (5.2) and later expressions the power gain and loss of switching stages and connections are not accounted for. This is for simplicity in logically modelling the PPM-HP router. The power gain and losses in the router will be discussed in Chapters 6 and 7.

The PPRT is initialised using a single pulse  $e(t) = (1 - 2\kappa)\text{Clk}(t + T_{\text{PPRT}})$ , which is recovered from the clock pulse, propagating through different delay units (see Chapter 6). The amplifier  $G_{\text{PPRT}}$  is used to maintain the power level of optical pulses in PPRT. The PPRT entries are expressed as:

$$E_m(t) = \sum_{d_m} e(t + d_m \times T_s), \quad \forall d_m \in D_m. \quad (5.3)$$

Each  $D_m$  set contains all of the decimal values of the address patterns assigned to the router output # $m$  ( $m = 1, 2, \dots, M$ ). If the equivalent decimal value of an incoming packet header address (i.e. target edge-node address) matches one element of the  $D_m$ , then the packet is switched to the router  $m^{\text{th}}$  output. Address correlations are carried out using an array of two-input optical AND gates, see Figure 5.2, with two inputs are  $E_m$  and  $a_{\text{PPM}}$  being amplified by  $G_{\text{AND}}$  to drive the SMZ-based AND gate. The correlation outputs are therefore given by:

$$mch_m(t) = a_{\text{PPM}}(t) \times E_m(t) = \begin{cases} 1 & \text{if } d_m = \sum_{i=1}^{N-1} a_i \times 2^i \quad \forall m \\ 0 & \text{if } d_m \neq \sum_{i=1}^{N-1} a_i \times 2^i \quad \forall m \end{cases}, \quad (5.4)$$

$$m = 1, 2, \dots, M \quad d_m \in D_m.$$

Only one bit-wise AND operation is required to carry out address correlation for each PPRT entry. Therefore the gain recovery issue of the SOA-based AND gate no longer affects to the speed of the header recognition. Since there is only a single pulse in the PPM frame  $a_{\text{PPM}}(t)$ , the matching pulse vector  $MCH(t) = [mch_1(t) \ mch_2(t) \ \dots \ mch_M(t)]$  for  $M$  PPRT entries has only one non-zero element in the unicast transmission mode.

Multiple-transmission mode can be implemented in the PPM-HP router. If there are more than one non-zero elements in  $MCH(t)$  due to pulses located in multiple PPRT entries, for example in positions 1 or 10 in Table 5.1, then the packet is switched to multiple outputs in the multicast transmission mode. If all entries have pulses at the 14<sup>th</sup> position, then the packet is broadcast to all  $M$  outputs of the core router.

For switching a short packet, where an OSW with a short SW is a requirement, a single matching pulse would be ideal. However, for switching long packets ( $\sim$  nanosecond length), the  $mch_m(t)$  is amplified (by  $G_{\text{CS}}$ ) and passed through an OSWC such as a multiple-pulse generator or all-optical flip-flop (AOFF) to obtain a  $CP_m(t)$  having multiple pulses or constant power, respectively, see Figure 5.2. This ensures that the gain of the  $SW_m$  in the OSW is flat during the switching duration. The switched packet  $PK_{\text{SW}}(t)$  for the  $m^{\text{th}}$  output is computed as:

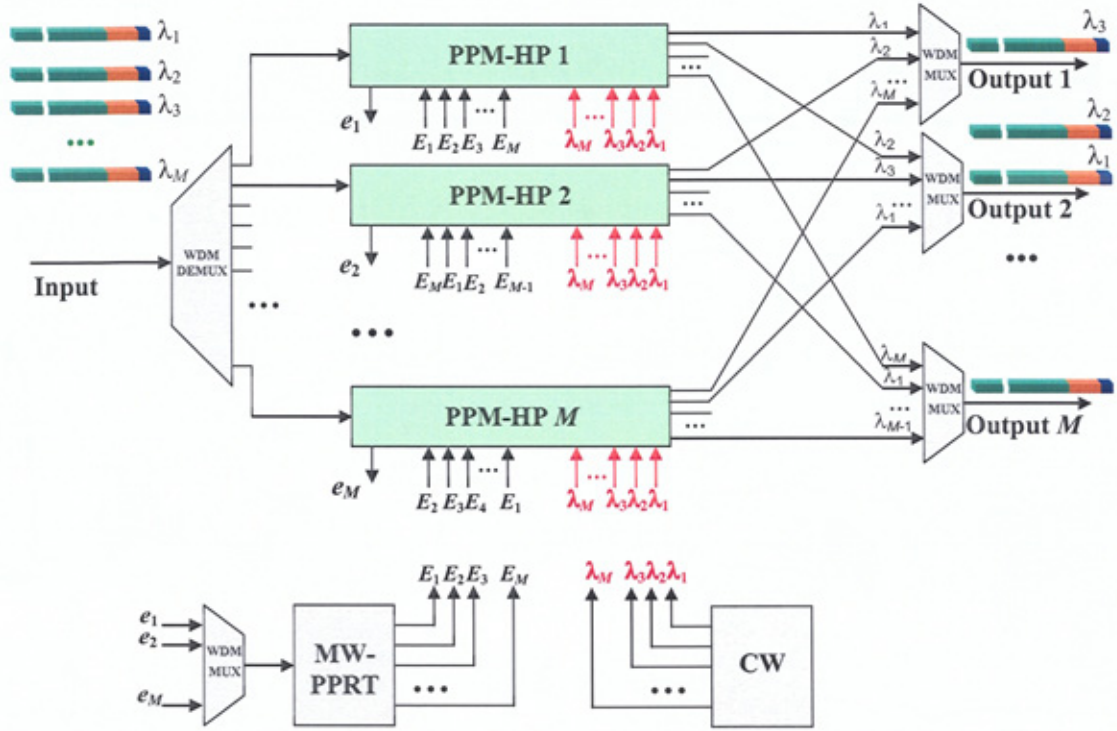
$$PK_{\text{SW}}(t) = PK(t + T_{\text{PPM-HP}}) \times mch_m(t), \quad (5.5)$$

where  $mch_m(t)$  is the resultant non-zero matching pulse.

#### 5.4.2 Multiple-wavelength PPM-HP router

The proposed PPM-HP router in Section 5.4.1 is used for single-wavelength input data packet(s). In the scenario where multiple packets at different wavelengths arrive to the router, the PPM-HP router should be capable of simultaneously processing and routing all the packets to the desirable outputs without any losses and delays (i.e. no congestion). In this section, the architecture of a  $1 \times M$  multiple-wavelength PPM-HP router (MW-PPM-HP router) is proposed to achieve all-optical routing transparency in WDM networks.

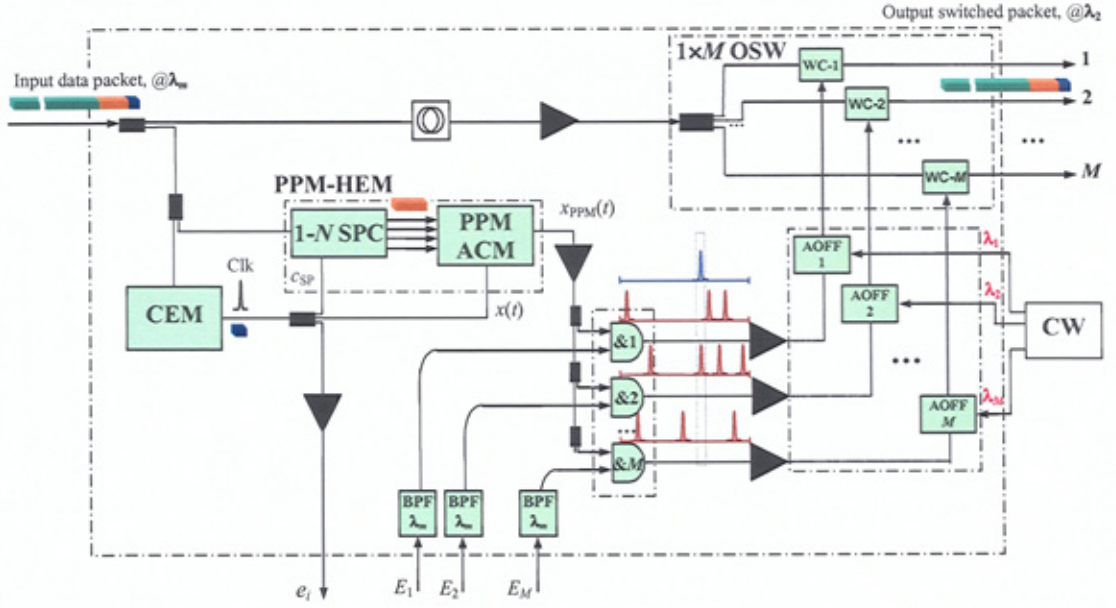
The proposed MW-PPM-HP router's block diagram is shown in Figure 5.4. The router comprises  $M$  PPM-HP modules in combination with a common MW-PPRT,  $M$  continuous wave (CW) laser sources and a number of WDM multiplexers and demultiplexers. At the router input,  $N$ -bit-address packets with multiple-wavelength (at  $\lambda_1, \lambda_2 \dots$  and  $\lambda_M$ ) are passed through a WDM demultiplexer before being fed to a bank of PPM-HP modules. Each PPM-HP module  $k$  ( $1 \leq k \leq M$ ) will process packets at a given wavelength  $\lambda_k$ . A single pulse  $e_k$  extracted from the clock pulse of the incoming  $\lambda_k$  packet in the  $k^{\text{th}}$  PPM-HP module is input to the MW-PPRT to generate  $M$  PPM-formatted routing table entries  $E_1, E_2, \dots, E_M$  (at the same  $\lambda_k$ ), which are then fed back to the  $k^{\text{th}}$  PPM-HP for address recognition.



**Figure 5.4** A block diagram of the proposed WDM  $1 \times M$  router based on PPM-HPs, a common MW-PPRT and assisted CW laser sources

Following the address correlation, in the  $k^{\text{th}}$  PPM-HP, the packet wavelength is converted to the wavelength  $\lambda_o$  ( $o = \text{modulo}(k + m - 1, M), \forall k, m, o \in [1, M]$ ) and the wavelength-converted packet is applied to the optical multiplexer to select the dedicated MW-PPM-HP router  $m$  output. To avoid PPM-HP modules from switching signals with identical wavelengths going to the same router output, permutations in feeding order of MW-PPRT entries to the inputs  $e_1, e_2, \dots, e_M$  of different PPM-HP modules are required, see Figure 5.4 and Figure 5.5. In the scenario when all  $M$  input packets are required to be switched to router output 1, there are up to  $M$  simultaneous signals at  $M$  different wavelengths emerging at each router output which offers a non-blocking characteristic of the proposed router.





**Figure 5.5** A diagram of a  $1 \times M$  PPM-HP router (operating at  $\lambda_k$ ) including wavelength converters showing the input packet at  $\lambda_m$  is converted to  $\lambda_2$  and switched to the PPM-HP output 2

Individual PPH-HP modules in the MW-PPM-HP router (see Figure 5.5) are constructed similarly to the router described in Figure 5.2, except for the external MW-PPRT, the replacement of the OSW by wavelength converters (WCs) and OSWC are AOFFs. The MW-PPRT stores the shortest-path information in the  $2^N \times M$  switching matrix by setting the appropriate delays and connections, see Figure 5.6(a). The single pulse  $e_k$  (at  $\lambda_k$ ) from the  $k^{\text{th}}$  PPM-HP module is applied to the MW-PPRT to generate  $M$  PPRT-entries  $E_1, E_2, \dots, E_M$ . In each entry  $E_m$  at  $\lambda_k$  ( $1 \leq m \leq M$ ) with a duration of  $2^N \times T_s$ , there are a number of pulses whose locations correspond to the decimal metrics of the address patterns assigned for the input packet being switched to the  $m^{\text{th}}$  output of the MW-PPM-HP router. An example of a MW-PPRT with  $N = 4$ ,  $M = 3$  is shown in Figure 5.6(b). In this MW-PPRT, if the incoming packet address matches with 0, 1, 2, 5, 8, 12, 14, or 0,

3, 7, 10, 13, 15 or 0, 1, 4, 6, 9, 11, the packet will be switched to the MW-PM-HP router output ports 1, 2 and 3, respectively. Similar to PPRT, when a pulse appears in the same location in more than one MW-PPRT entry, the incoming packet is switched to multiple router outputs (i.e. multicast and broadcast).

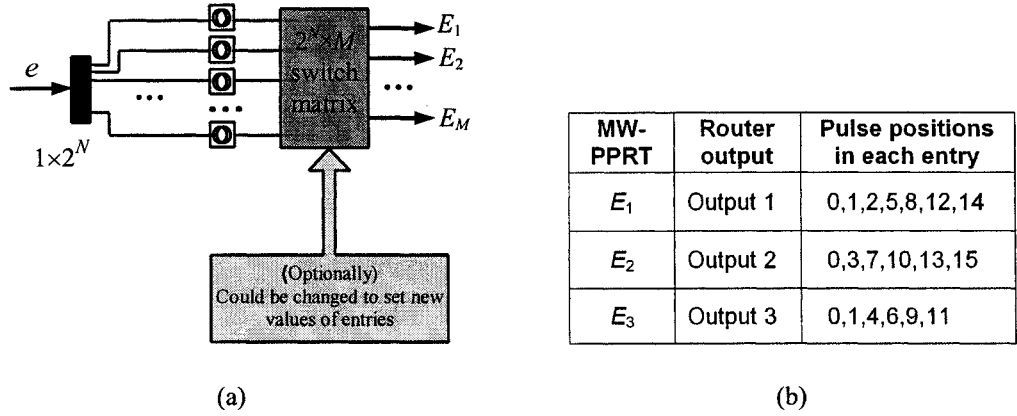


Figure 5.6 (a) A diagram of MW-PPRT and (b) MW-PPRT for  $N=4$ ,  $M=3$

The matching output from the  $o^{\text{th}}$  AND gate of the  $k^{\text{th}}$  PPM-HP is applied to set the  $o^{\text{th}}$  AOFF on. In this thesis, high-speed SMZ-based wavelength converters are adopted from the work reported in [157] which requires a constant signal (or continuous wave CW) to operate. The constant signal from the  $o^{\text{th}}$  AOFF output will have a duration equivalent to the packet duration  $T_{\text{pk}}$  where its wavelength is  $\lambda_o$ . This CW will incorporate with input packet using the XPM effect (Figure 3.7(b)) in WC- $o$  to switch the packet to the  $o^{\text{th}}$  output port of the  $k^{\text{th}}$  PPM-HP module. Outputs of individual PPM-HP modules will be wavelength multiplexed to the dedicated router output port.

## 5.5 Summary

Chapter 5 introduced the PPM concept applied for high-speed all-optical routing for single and multiple wavelength transmission. The proposed PPH-HP offers a number of features:

- Reduces the number of routing table entries through the introduction of PPRT, thus reducing the header recognition speed
- Overcomes the header recognition speed limitations induced by slow response-time and recovery-time of existing all-optical AND gates based on the SOA, by using only a single bit-wise AND operation for the entirely exhaustive correlation
- Offers good scalability, i.e. updating the PPRT when adding/dropping additional routers/nodes or increasing/decreasing packet header address length ( $N$ ) will not alter the total number  $M$  PPRT entries, as  $M$  is the number of router outputs
- Offers unicast, multicast and broadcast transmission-mode capabilities embedded in the optical domain (i.e. physical layer).

The concepts of single-wavelength and multiple-wavelength PPM-HP routers were first introduced in publications [A22] and [A14], respectively. The details and investigations of the outlined router elements and router performance will be presented in Chapters 6 and 7 with further specific publications.



## CHAPTER 6

### PPM-HP ROUTER MODULES

#### 6.1 Introduction

The proposed  $1 \times M$  PPM-HP router includes key modules such as clock extraction, PPM header extraction, PPRT, a bank of all-optical AND gates, an optical switching controller and a  $1 \times M$  optical switch. Firstly, the CEM, a vital module extracting clock pulse for the synchronisation of data packet arrival and the router operation, is introduced. The extracted clock pulse is used to drive the PPM-HEM for converting the packet header address to a PPM-address and to generate the PPRT entries, which is discussed next. The outputs of these modules are compared using a bank of all-optical SMZ-based AND gates with only single bit-wise operation being required. Optical switching unit are presented, including the  $1 \times M$  optical switch and optical switching controller, for ensuring a constant switching gain at the router output. In each section, the module operation principle is first presented, followed by investigation of its characteristic.

## 6.2 Clock Extraction Module

The rapid increase of internet and multimedia services in recent years is a driving force for the developments of high-speed optical systems. Clock extraction (clock recovery) plays a significant role in providing proper optical system operation or making an accurate test measurement, whether as a part of an optical system or incorporated into a test-bed, respectively. Different architectures that exist for achieving clock extraction in the optical domain have been reviewed in Section 2.3.1. As discussed, a new scheme for ultrafast clock extraction based on two inline SMZ switches is proposed in this thesis, due to its fast response and low-complexity properties.

### 6.2.1 Operation principle

Figure 6.1 shows a schematic block diagram of the proposed CEM employing two inline SMZs. The arriving packet is directed to the input of SMZ-1 after being delayed by  $T_{SW}/2$ . Two amplified (by a gain  $G_{CP}$ ) versions of the arriving packet, one with no delay and the other delayed by  $T_{SW}$ , are fed into the control ports as  $CP_1$  and  $CP_2$ , respectively. The control and input signals applied to each SMZ are set in an orthogonal-polarisation state by a PC and are separated by a PBS at the SMZ output. With no CPs ( $CP_1$  and  $CP_2$ ) at locations (b) and (d) the SMZ-1 is in the balanced state (both SOAs gains and phases are identical) resulting in no signal at its output port (e). In the presence of CPs SMZ-1 is in the imbalanced state (i.e. transmitting mode) and has a SW width of  $T_{SW}$ , thus allowing the input signal to emerge from its output port, see point (e). The time delay  $T_{SW}$  is selected smaller than a single bit duration  $T_b$ , thus only extracting the clock bit using SMZ-1.



CPs, the gains of the SOAs in SMZ-1 will drop. However, as both CPs are amplified packets containing random “0” and “1” bits, the SOA gain starts to recover during bit “0”s since no CPs are present. Successive binary “1”s in the CPs will again create their new residual SW, thus allowing it to emerge at the output of SMZ-1 following the extracted clock bit, see location (e) in Figure 6.1. However the intensities of these residual bits “1” are lower than the intensity of the extracted clock bit due to the SOA gain recovery time being typically much greater than the relatively small  $T_b$  in high-speed networks (i.e.  $T_b \sim$  picoseconds) resulting in low residual SW gain.

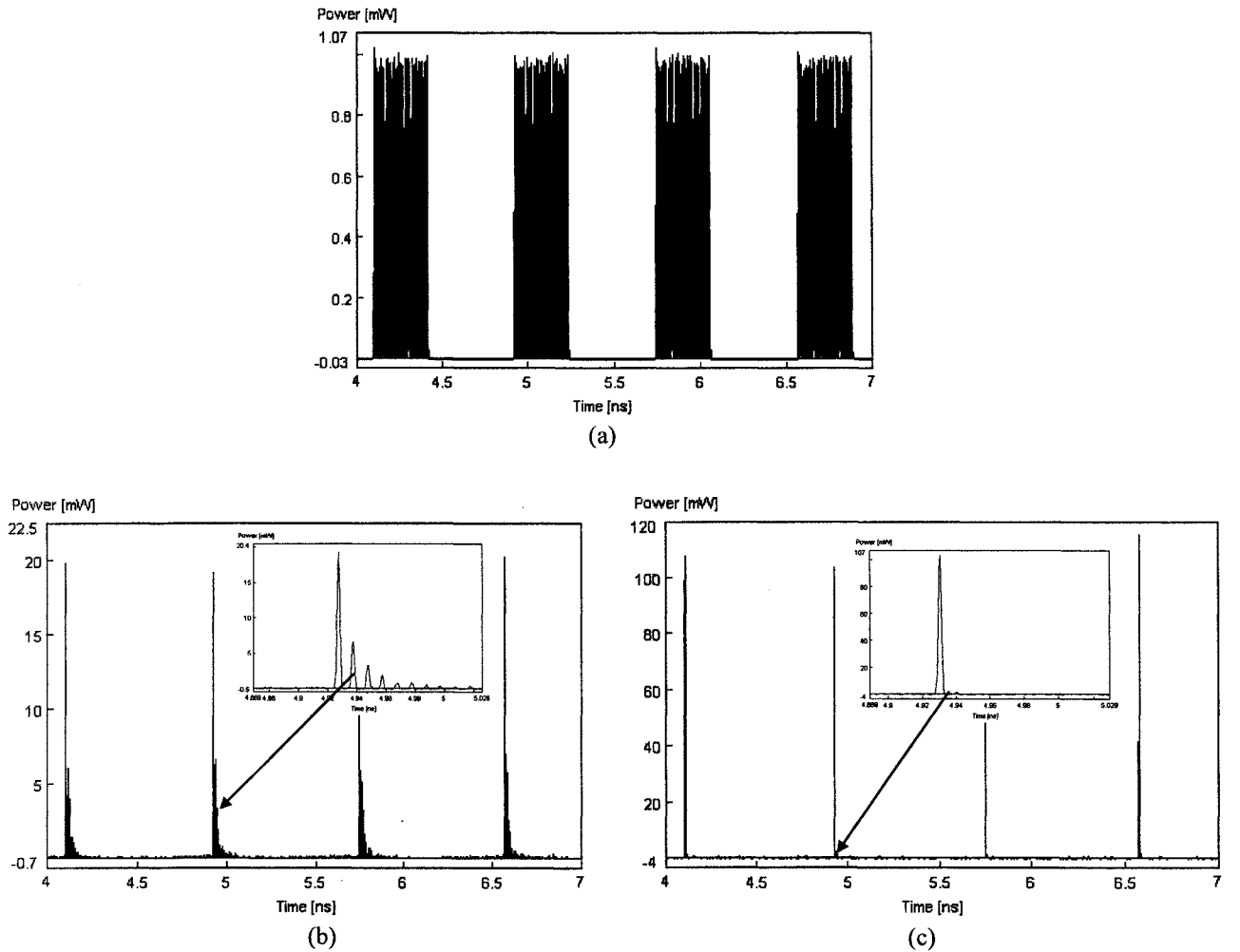
In order to suppress the residual signals at the output of SMZ-1 and achieve a higher *CR* in clock extraction, a SMZ is used in cascade (i.e. SMZ-2 with SMZ-1). The extracted signals from SMZ-1 are used in SMZ-2 with the same input/control configurations as in SMZ-1 except for differently chosen input/control powers. The CPs (shown at points (f) and (h)) in SMZ-2 will create a main SW to extract the clock pulse with a high intensity at the output of SMZ-2. Note that due to low-intensity residual signals appearing at the input (at (g)) and control ports of SMZ-2, the gain of the main SW is much larger than the gain of the newly generated residual SWs. As a result, the intensity of the residual signals at the CEM output, see location (i), is further reduced in comparison to the extracted clock pulse.

**Table 6.1** CEM parameters for simulation

Parameters	Values
Input data bit rate	100 Gbit/s
Bit duration - $T_b$	10 ps
Packet guard band	0.5 ns
Data pulse (peak) power	0 dBm
Data pulse width - FWHM	2 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Switching window width - $T_{sw}$	6 ps
SSMF length	30 km
DCF length	5 km
SMZ-1 amplifier gain - $G_{CP}$	9 dB
SMZ-2 attenuation - $\alpha$	12 dB
SOA length - $L_{SOA}$	$500 \times 10^{-6}$ m
SOA active region width	$3 \times 10^{-6}$ m
SOA active region height	$80 \times 10^{-9}$ m
Linewidth enhancement factor - $\alpha_{LEF}$	4
Confinement factor - $\Gamma$	0.2
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup>
Internal losses	$40 \times 10^2$ m <sup>-1</sup>
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Group velocity - $V_g$	$3 \times 10^8$ / 3.5 ms <sup>-1</sup>
Effective DC injection current - $I_e$	0.15 A
Recombination coefficient A	$1.43 \times 10^8$ s <sup>-1</sup>
Recombination coefficient B	$1 \times 10^{-16}$ m <sup>3</sup> s <sup>-1</sup>
Recombination coefficient C	$3 \times 10^{-41}$ m <sup>6</sup> s <sup>-1</sup>

Simulations are carried out using the VPI simulation software to confirm the operation and investigate *CR* performance of the proposed CEM. The simulation parameters adopted are given in Table 6.1 for the CEM and SOA. The transmitted packet comprises of Gaussian pulses for the clock and payload bits. There is an inter-packet guard band of

0.5 ns for SOA gain recovery. The gain of the SOA model is assumed to be polarisation independent. Figure 6.2(a) shows a packet stream at the input to the CEM. The extracted clock pulse and residual signals at the output of SMZ-1 are shown in Figure 6.2(b) with the given values of  $G_{CP}$  and  $T_{SW}$  in Table 6.1. In the inset multiple residual pulses spread over several bit intervals, due to the lower-gain residual switching windows of SMZ-1, are clearly visible. The achieved  $CR$  is 5 dB.



**Figure 6.2** (a) Input data packets, (b) extracted clock pulse at the SMZ-1 output, (c) extracted clock pulse at the SMZ-2 (i.e. CEM) output with reduced residual signals

Figure 6.2(c) shows a high intensity extracted clock pulse at the output of SMZ-2 (i.e. at the CEM output). It is shown that the  $CR$  is much improved to  $\sim 18$  dB. The suppression of residual signals is implemented by cascading SMZs, see the inset of Figure 6.2(c) compared to Figure 6.2(b). Note that the high intensity of the extracted clock pulse is due to the signal being amplified by the SMZs (SMZ-1 and SMZ-2).

The actual CEM processing time is dictated by the dedicated delay of  $2 \times T_{in}$  in addition to the actual time required for packet propagation through both SMZ stages.

### 6.2.2 Extracted clock contrast ratio

The contrast ratios (in dB) against the input packet pulse energy for different values of  $G_{CP}$  for a single SMZ-1, and the complete CEM module are illustrated in Figure 6.3.

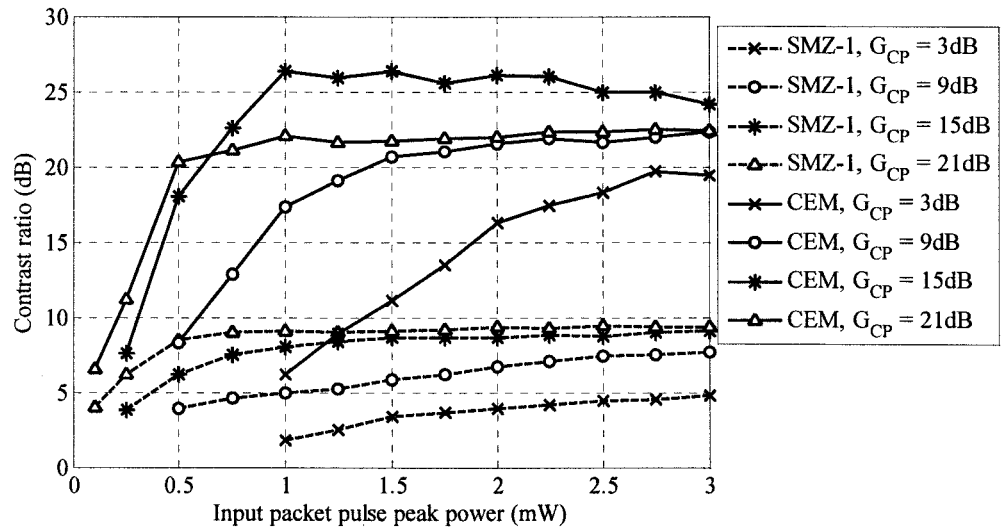


Figure 6.3 Contrast ratio against the range of input packet pulse power for different values of  $G_{CP}$

For the single SMZ-1 stage having  $G_{CP} = 3$  dB, the lowest  $CR$  ( $< 5$  dB) is observed.  $CR$  is improved with high values of  $G_{CP}$  and input packet pulse power because of the lower gain of the residual switching windows as a result of a deeper SOA gain saturation by the CPs. Beyond a  $G_{CP}$  of 21 dB no further improvement in  $CR$  performance ( $\sim 10$  dB) can be achieved. At the output stage of the CEM (i.e. SMZ-2),  $CR$  significantly improves with an increase in  $G_{CP}$  and input packet pulse power, reaching a maximum value of 27 dB at the  $G_{CP}$  and input power values of 15 dB and 1 mW, respectively. However, further increases in either  $G_{CP}$  ( $\geq 21$  dB) or input energy will result in a reduction in  $CR$ . This reduction is due to the decreased gain of the main switching window when SOAs are deeply saturated.

## 6.3 PPM Header Extraction Module

### 6.3.1 Operation principle

The operation principle of PPM-HEM was described in Chapter 5. This section will present an in-depth characterisation and investigation of the module performance. Figure 5.3 showed the HEM diagram including SPC and PPM-ACM. The SPC is composed of  $N$ -single SMZ switches which open narrow switching windows to extract the individual address bits  $a_i$  ( $1 \leq i \leq N$ ). The parallel single address bits extracted by the SPC are amplified and delayed for use as the high-powered control signals in the PPM-ACM. For the SPC, all switches should have a high contrast ratio  $CR_{CH1}$  (Section 4.2.1) to ensure reduced residual power residing outside the SW with the width of  $T_{SW}$  (i.e. low crosstalk). The residual power can be suppressed by employing the unequal power



control-pulse scheme, provided that the incoming packets have constant power levels as presented in Section 4.2. In case the incoming packets have non-constant power levels and  $T_{\text{SW}}$  is small (a few picoseconds), due to the patterning effect discussed in Section 3.2, both  $\text{CP}_1$  and  $\text{CP}_2$  have equal power resulting a small amount of  $\text{RCXT}$  presenting at the SPC output ports (see Figure 4.5 with  $R = 0$  dB and  $T_{\text{SW}} = 5$  ps).

PPM-ACM is implemented by means of propagating the clock pulse  $\text{CP}_{\text{PPM-ACM}}(t)$  through  $N$   $1 \times 2$  switching stages. The switching stage  $i$  will receive the amplified and delayed  $a_i$  as the control pulse. At the input to the PPM-ACM (i.e. the first switching stage) the single pulse  $\text{CP}_{\text{PPM-ACM}}(t)$  is applied right after all  $a_i$  excited switching stages. In PPM-ACM, a  $1 \times 2$  switch is employed having low  $\text{CR}_{\text{CH}j}$  and  $\text{CR}_{\text{OP}ij}$  ( $i = 1$  and  $2$ ) resulting in high intra-channel crosstalk at its output ports, thus leading to multiple pulses emerging at the output of the PPM-ACM with different delays in addition to the desired PPM pulse  $a_{\text{PPM}}(t)$ . Based on the investigation carried out in Section 4.2 for a single  $1 \times 2$  SMZ switch, the achieved  $\text{CR}_{\text{CH}1}$  is  $\sim 20$  dB which is much better than  $\text{CR}_{\text{CH}2}$  (see Figure 4.8), thus one needs to improve  $\text{CR}_{\text{CH}2}$  and  $\text{CR}_{\text{OP}12}$  to ensure satisfactory PPM-HEM operation. The proposed TaMZ switch is suitable for this application; however, in term of energy dissipation (due to the use of a constant bias optical signal) and the complexity (using an additional AOFF), it is desirable to develop a high contrast-ratio  $1 \times 2$  switch with a low energy operation and decreased complexity.

Here the proposed  $1 \times 2$  switch is based on two SMZs (see Figure 6.4) offering higher output  $\text{CR}$  at both outputs without the need for the bias signal.



switch's  $OP_2$ . With a control pulse  $CP_{SMZ1}$  is applied to SMZ-1, see Figure 6.4(b), the input pulse emerges at  $OP_1$  of SMZ-1, i.e.  $1 \times 2$  switch  $OP_1$ . However a residual signal also emerges at  $OP_2$  of SMZ-1 (further details were discussed in Section 4.3). To ensure that no signal emerges at the  $1 \times 2$  switch  $OP_2$ , a portion of the output pulse at SMZ-1  $OP_1$  is amplified and used as an identical pair of control pulses  $CP_{SMZ1-OP1}$  simultaneously applied to SMZ-2. When  $CP_{SMZ1-OP1} \gg CP_{SMZ1-OP2}$ , the SMZ-2 switch is in the balanced state, due to  $CP_{SMZ1-OP1}$ , therefore no signal will emerge from  $OP_1$  of SMZ-2 (i.e. the  $1 \times 2$  switch  $OP_2$ ).

The attenuator (Attn.) in Figure 6.4(a) and (b) is used for two purposes: (i) reducing the power for  $CP_{SMZ1-OP2}$  when  $CP_{SMZ1}$  is not applied to ensure that SMZ-2 is in self-switching mode but SOAs are not oversaturated, and (ii) ensuring  $CP_{SMZ1-OP2}$  intensity to be sufficiently smaller than  $CP_{SMZ1-OP1}$ .

### 6.3.2 $1 \times 2$ switching stage inter-output contrast ratio

The performance of the PPM-HEM is evaluated by investigating the individual switching-stage gain and  $CR$ . This is necessary because propagation of the  $CP_{PPM-ACM}$  pulse through multiple  $1 \times 2$  switching stages in the PPM-ACM will result in multiple pulses at the PPM-HEM output. If the intensities of these unexpected multiple pulses are relatively high, then they would result in false matching of the converted PPM address with wrong slots in the PPRT entries at different AND gates. Thus the incoming packet could be switched to multiple router output ports including the intended and unintended

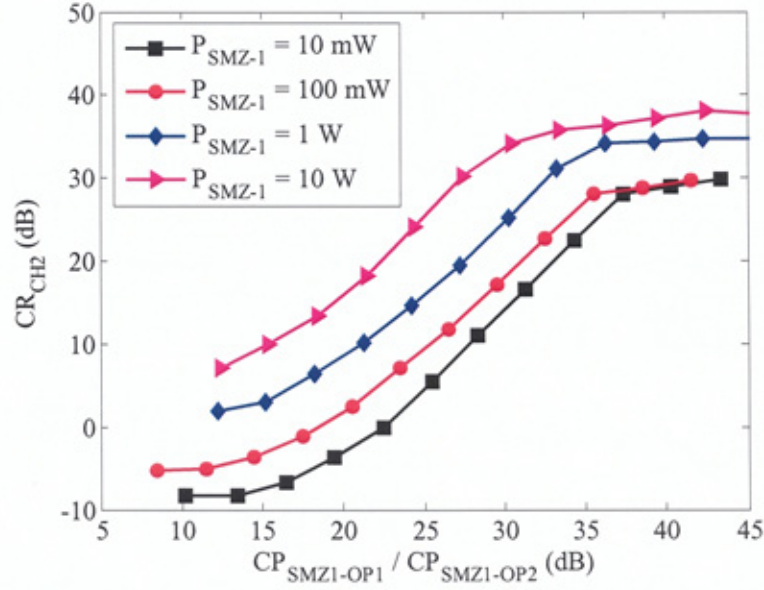
ports. There are two contributors to the multiple-pulse effect: (i) low  $CR_{CH1\&2}$  and (ii) low  $CR_{OP12}$ .

**Table 6.2** 1×2 two-SMZ based switch parameters

Parameters	Values
Data pulse (peak) power	0 dBm
Data pulse width - FWHM	2 ps
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Attenuation - Attn	12 dB
CP (peak) power - $P_{SMZ1}$	10 dBm, 20 dBm, 30 dBm, 40 dBm (10mW, 100mW, 1W, 10 W)
SOA length - $L_{SOA}$	$500 \times 10^{-6}$ m
SOA active region width	$3 \times 10^{-6}$ m
SOA active region height	$80 \times 10^{-9}$ m
Linewidth enhancement factor - $\alpha_{LEF}$	4
Confinement factor - $\Gamma$	0.2
Differential gain - $g_d$	$2.78 \times 10^{-20}$ m <sup>2</sup>
Internal losses	$40 \times 10^2$ m <sup>-1</sup>
Carrier density at transparency - $N_T$	$1.4 \times 10^{24}$ m <sup>-3</sup>
Group velocity - $V_g$	$3 \times 10^8$ / 3.5 ms <sup>-1</sup>
Effective DC injection current - $I_e$	0.15 A
Recombination coefficient A	$1.43 \times 10^8$ s <sup>-1</sup>
Recombination coefficient B	$1 \times 10^{-16}$ m <sup>3</sup> s <sup>-1</sup>
Recombination coefficient C	$3 \times 10^{-41}$ m <sup>6</sup> s <sup>-1</sup>

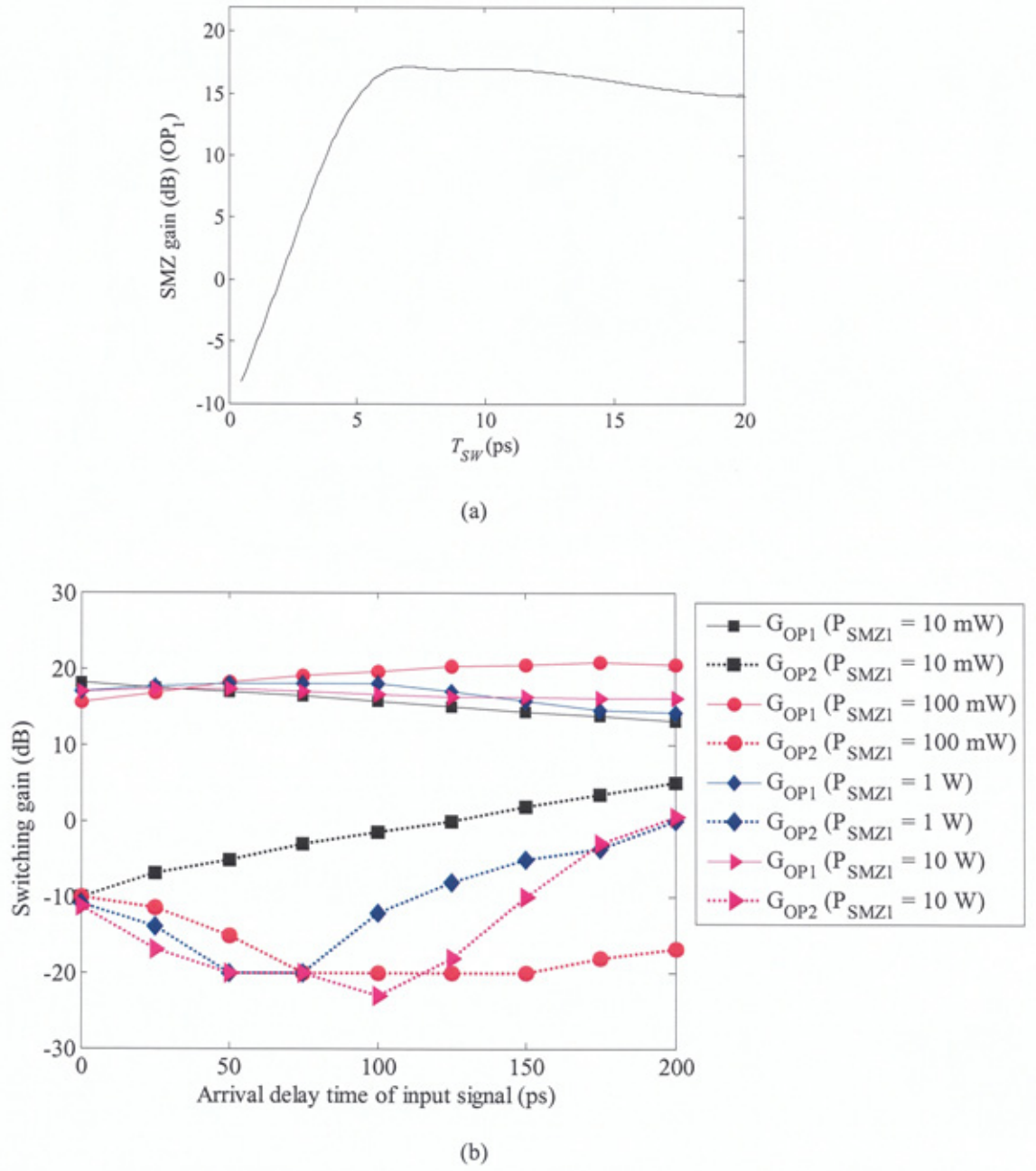
Figure 6.5 shows the simulated  $CR_{CH2}$  for the proposed 1×2 switch with the parameters given in Table 6.2. It is noticed that compared to Figure 4.8,  $CR_{CH2}$  is much improved with the increase of the power ratio of  $CP_{SMZ1-OP1} / CP_{SMZ1-OP2}$ . Also for  $CP_{SMZ1}$  with high power  $P_{SMZ1}$  the improvement of  $CR_{CH2}$  is noticeable in comparison to the lower

$CP_{SMZ1}$  powers. These could be explained by the improved balance achieved in SMZ-2 when a higher power of  $CP_{SMZ1}$  is applied thus resulting in a higher power of  $CP_{SMZ1-OP1}$ .



**Figure 6.5** Simulated  $CR_{CH2}$  against the normalised  $CP_{SMZ-OP1}$  for  $1 \times 2$  switch based on two SMZ switches for a range of  $P_{SMZ-1}$

Figure 6.6(a) shows the gain of the SMZ switch with respect to the switching window width  $T_{SW}$ . The gain increases with  $T_{SW}$ , reaching a maximum value of  $\sim 17$  dB at  $T_{SW}$  of  $\sim 7$  ps. Note that typically the SOA gain is 26 dB, therefore the maximum SMZ gain is 17 dB due to the use of the  $2 \times 2$  3-dB input, control and output couplers (i.e. 9 dB insertion loss). Beyond this point the gain decreases, due to the SOA gain recovery in the SMZ. For larger  $T_{SW}$ ,  $RCXT$  will be increased, whereas smaller  $T_{SW}$  will result in reduced signal intensity.



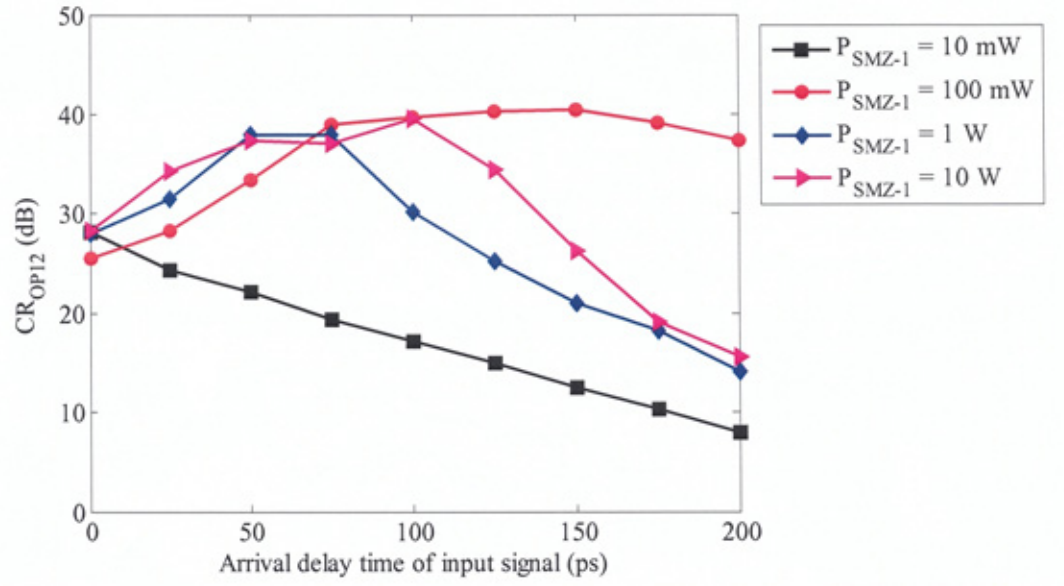
**Figure 6.6** (a) SMZ gain against  $T_{SW}$  and (b)  $1 \times 2$  two-SMZ-based switch gain at both outputs against the arrival delay of input signal to the switch (when  $CP_{SMZ1}$  is applied with different  $P_{SMZ1}$ )

For a  $1 \times 2$  two-SMZ based switch, the switching gains shown in Figure 6.6(b) are observed at output ports 1 and 2 against the arrival delay of input signal with different

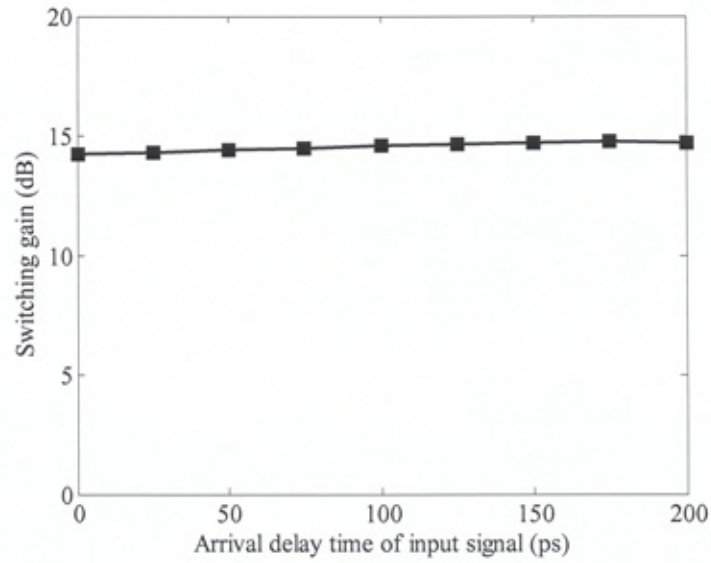
values of  $P_{\text{SMZ1}}$ . Note that the switching operation is initialised by applying a single narrow control pulse  $CP_{\text{SMZ1}}$  to the switching stage, i.e. the extracted address bit  $a_i$ . The switching gain at output 1 is gradually decreased with the input pulse arrival delay increase due to the SOA gain recovery in SMZ-1 after the single pulse  $CP_{\text{SMZ1}}$  exits SMZ-1. In contrast, further SOA gain recovery with a longer input pulse arrival delay will result in a greater imbalance in SMZ-2. Therefore the switching gain at output 2 will increase. For each  $P_{\text{SMZ1}}$ , the power ratio of  $CP_{\text{SMZ1-OP1}} / CP_{\text{SMZ1-OP2}}$  is set such that the achieved  $CR_{\text{CH2}}$  is around 25 dB referenced to Figure 6.5.

The resultant inter-output  $CR$  is illustrated in Figure 6.7(a). The achieved  $CR_{\text{OP12}}$  is high when the delay is small. In the region of 50 to 150 ps,  $CR_{\text{OP12}}$  is increased due to the high switching gain at  $\text{OP}_1$  and low residual gain at  $\text{OP}_2$ . However, when this delay is long (i.e.  $> 150$  ps), the contrast ratio is reduced due to SMZ-1 and SMZ-2 gain recoveries. For a low  $P_{\text{SMZ1}}$  (10 mW),  $CR_{\text{OP12}}$  is rapidly reduced because the SOAs are not deeply saturated resulting in a quick gain recovery. When  $P_{\text{SMZ1}}$  is around 100 mW, the achieved  $CR$  is increased. However higher values of  $P_{\text{SMZ1}}$  will deeply saturate SMZ-1 resulting in the low power of  $CP_{\text{SMZ1-OP1}}$  and in turn the gains of the SOAs in SMZ-2 are quickly recovered, see Figure 6.7(a). Figure 6.7(b) shows the switching gain of the output 2 of the proposed  $1 \times 2$  switch. It is shown that the gain is invariant along with the arrival of an input pulse as long as the input power and  $1 \times 2$  switch specifications are fixed. Note the gain of output 1 of the proposed  $1 \times 2$  switch is not shown since no signal is switched by SMZ-1 to its  $\text{OP}_1$  in the absence of the  $CP_{\text{SMZ1}}$ .





(a)



(b)

**Figure 6.7** (a) The resultant  $CR_{OP12}$  against the arrival delay of input signal to the switch. The arrival delay is measured from the time  $CP_{SMZ1}$  being applied and the time  $CP_{PPM-ACM}$  arriving to PPM-ACM and (b) switching gain of output 2 of a  $1 \times 2$  two-SMZ-based switch when no  $CP_{SMZ1}$  is applied.



### 6.3.3 PPM-HEM multiple-pulse output and on/off contrast ratio

At the 1<sup>st</sup> switching stage, the  $CP_{\text{PPM-ACM}}$  pulse is switched to either  $OP_1$  or  $OP_2$ , see Figure 5.3. The  $CP_{\text{PPM-ACM}}$  signal is also leaked to the either  $OP_2$  or  $OP_1$ , respectively, because of the non-zero  $CR_{OP12}$ . Since  $OP_1$  and  $OP_2$  are connected, the switched  $CP_{\text{PPM-ACM}}$  pulse and the leaked pulse are temporally multiplexed, thus resulting in the appearance of an additional pulse with  $CP_{\text{PPM-ACM}}$ . Propagation of these pulses through subsequent switching stages will result in the generation of unwanted pulses in the same manner as in previous states due to the switch's non-zero  $CR_{OP12}$ . This would lead to the emergence of multiple pulses at the PPM-HEM outputs [204]. The number of generated pulses at the PPM-HEM output (excluding of  $CP_{\text{PPM-ACM}}$ ) is calculated as:

$$N_{\text{PPM-HEM}} = 2^N - 1. \quad (6.1)$$

From (6.1) it is shown that the generated pulses and  $CP_{\text{PPM-ACM}} \left( t + \sum_{i=0}^{N-1} a_i \times 2^i \times T_s \right)$  occupy all  $2^N$  slots of the PPM frame  $a_{\text{PPM}}(t)$ . If the intensity of an undesired pulse is sufficiently high, the matching pulse in (5.4) is not unique, thus resulting in switching the incoming packet to the wrong router output. This will be investigated further in Chapter 7.

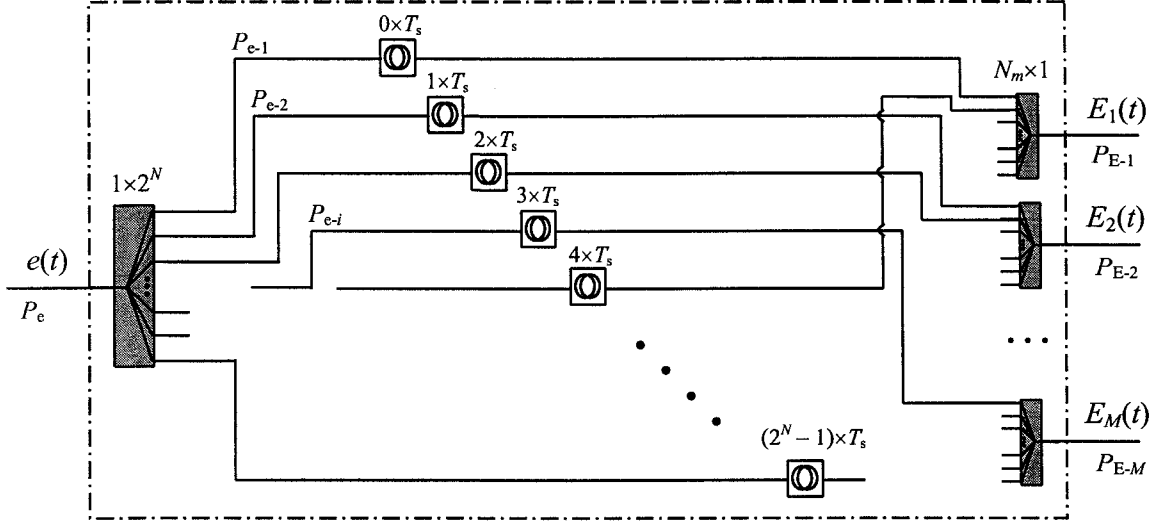
As shown in Figure 6.6(b) and Figure 6.7(b), gains at outputs 1 and output 2 in switching and non-switching modes, respectively, are approximately flat over a range of the arrival delay. It is advantageous that the net gain of each stage is normalised to unity

to ensure correct operation of a switching stage. As a result, the on/off  $CR$  of  $a_{\text{PPM}}(t)$  signal is equivalent to the  $CR_{\text{OP12}}$  of the last switching stage.

Note that the arrival time of  $CP_{\text{PPM-ACM}}$  to the  $i^{\text{th}}$  intermediate  $1 \times 2$  switch could be varied due to the bit pattern (“0”s or “1”s) of the packet header address  $a_{i-1}, a_{i-1}, \dots, a_0$ . Therefore  $CR_{\text{OP12}}$  will change with the arrival delay, see Figure 6.7(a), resulting in an increase in crosstalk level at the PPM-HEM output when  $N$  is large. In order to ensure high  $CR_{\text{OP12}}$  regardless of the arbitrary arrival delay, the control signal for each  $1 \times 2$  switch could be either (i) a multiple high-powered pulse stream or (ii) a continuous constant-power signal instead of an amplified single pulse  $a_i$ . The required duration of the new control signal should be as long as half of the PPM-address conversion time, i.e.  $T_{\text{CP-HEM}} = 0.5 \times 2^N \times T_s$ . Further details of multiple-pulse stream generation and continuous constant-power signal produced by AOFF will be discussed in Sections 6.6.1 and 6.6.2, respectively.

## 6.4 Pulse Position Routing Table Generation

PPRT is mathematically described in (5.3) and its architecture is illustrated in Figure 6.8. The PPRT optical circuitry comprises of a  $1 \times 2^N$  splitter, up to  $2^N$  delay units and  $M$   $N_m \times 1$  combiners, where  $N_m$  is the total number of pulses in  $E_m$  (Section 5.3).



**Figure 6.8** Pulse-position routing table architecture based on splitter, delay units and combiner

To generate  $M$  PPRT entries, the input pulse  $e(t)$  is passed through the  $1 \times 2^N$  splitter, the output of which is delayed before being recombined. A maximum number  $N_{m,\text{tot}}$  of  $2^N$  delay paths is required for PPRT generation when the conventional routing table contains all  $2^N$  possible entries. Assuming that the input power is  $P_e$ , the power (in dB) of the  $i^{\text{th}}$  delay path  $P_{e-i}$  (in dB) is given as:

$$P_{e-i}(\text{dB}) = 10\log_{10}(P_e) - L_{\text{excess}} - 10\log_{10}(N_{m,\text{tot}}), \quad (6.2)$$

where  $L_{\text{excess}}$  (in dB) is the excess loss due to the insertion loss of the splitter and is defined as:

$$L_{\text{excess}} = 10\log_{10}\left(\frac{P_{\text{in-t}}}{P_{\text{out-t}}}\right), \quad (6.3)$$

where  $P_{\text{in-t}}$  and  $P_{\text{out-t}}$  are the total input and output powers, respectively. Assuming that the combiner output  $E_m$  has  $N_m$  dedicated bit “1”s (i.e.  $N_{m,\text{tot}} = \sum_{m=1}^M N_m$ ), the output power  $P_{E-m}$  (in dB) is given as:

$$P_{E-m}(\text{dB}) = 10 \log_{10}(P_{e-i}) - L_{\text{excess}} - 10 \log_{10}(N_m). \quad (6.4)$$

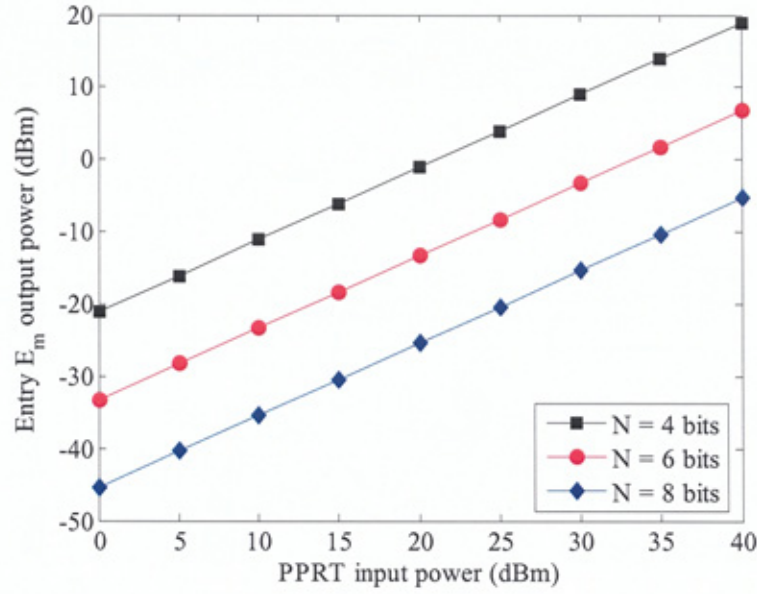
Substituting for  $P_{e-i}$  from (6.2) results in:

$$P_{E-m}(\text{dB}) = P_e(\text{dB}) - L_{\text{PPRT}}, \quad (6.5)$$

where the total power loss due to PPRT  $L_{\text{PPRT}}$  (in dB) is determined by:

$$L_{\text{PPRT}} = 2L_{\text{excess}} + 10 \log_{10}(N_{m,\text{tot}}) + 10 \log_{10}(N_m). \quad (6.6)$$

Figure 6.9 plots the linear input/output power characteristic for a range of  $N$ ,  $L_{\text{excess}}$  of 1 dB [205],  $M$  is 3 (router outputs),  $N_{m,\text{tot}}$  is  $2^N$  and  $N_m$  is  $N_{m,\text{tot}}/M$ . Note that a high input power  $P_e$  is required for a high value of  $N$  due to the assumption of a full-entry routing table, which results in a high value of  $L_{\text{PPRT}}$  in (6.6). If  $N_{m,\text{tot}} < 2^N$ , i.e. the routing table is not full-entry, or an address represents a range of addresses (see Chapter 8), then the required  $P_e$  is reduced.



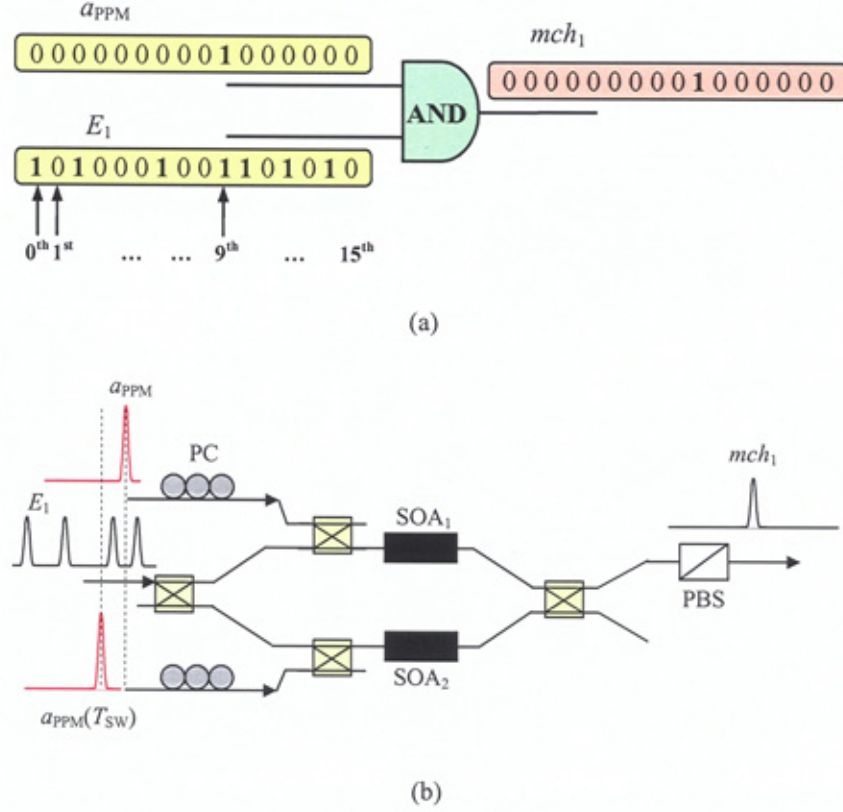
**Figure 6.9** Input power  $P_e$  against output power of the  $m^{\text{th}}$  PPRT entry  $P_{E-m}$  for a range of  $N$  bits

An alternative approach to construct a PPRT with reduced size compared to a very large conventional routing table with tens of thousands of entries (in IP over WDM) is to use a programmable optical-pulse pattern generator. However, with this approach one needs to use the extracted optical clock pulse as the trigger signal for pattern instigation. In this thesis, PPRT, based on the proposed passive structure, would be the preferred choice, as the router demonstration and its performance investigation are limited for small  $N$ .

## 6.5 Single-Bitwise AND Gates

$M$  2-input AND gates are required to carry out correlations between the PPM-address  $a_{\text{PPM}}(t)$  and  $M$  PPRT entries  $E_m(t)$ . Figure 6.10(a) illustrates an example for  $E_1$  (in Table 5.1) and  $a_{\text{PPM}}(t)$  with a pulse located at its slot 9. The correlated output  $mch_1(t)$  shows a single pulse at the 9<sup>th</sup> position. To implement a 2-input AND operation, there is a

number of techniques based on all-optical switches including TOAD, UNI and SMZ switches. Amongst these, SMZ types offer the best performance in speed, power consumption and integration capability as outlined in Section 2.4.



**Figure 6.10** (a) Correlation of  $a_{PPM}$  and  $E_1$  and (b) single bit-wise AND gate based on SMZ switch

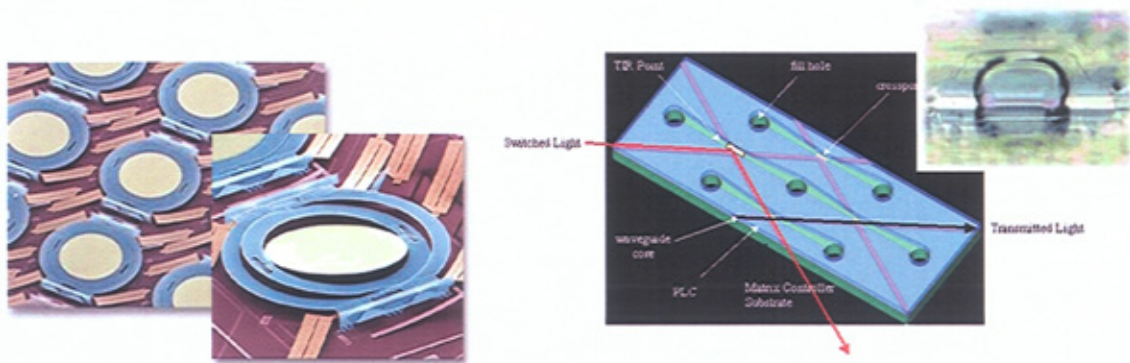
Figure 6.10(b) illustrates the configuration of the SMZ-based AND gate with two inputs of  $a_{PPM}(t)$  and a  $E_m$ .  $a_{PPM}(t)$  signal with a high intensity used as the CP to open and close the switch at the required PPM slot position, to switch the bit in  $E_m$  (at the same slot position). Therefore, only one single bit-wise AND operation is required. The SW width  $T_{SW} \leq T_b$  is set by the delay between two CPs. Since SMZ has a narrow SW as small as 1 ps, the achieved processing speed could be very high, i.e. by choosing a very short slot



duration  $T_s$ .  $a_{PPM}$  and  $E_1$  are set in orthogonal polarisations and separated at the SMZ output by a PBS.

## 6.6 Optical Switch Controller and $1 \times M$ Optical Switch

Optical switches can be categorised by their scale and response speed. For a large scale multiple input-output switching fabric, i.e.  $8 \times 8$ ,  $16 \times 16$  or  $32 \times 32$  switches, there is a number of commercial approaches including an array waveguide grating (AWG), Bubble switch (Agilent Tech Inc.) and micro-electromechanical systems (MEM) manufactured by Lucent Technology. Although these devices switch the packets optically without O-E-O conversion, their responses are typically as slow as microseconds or milliseconds. This is due to the required time for injecting bubbles, or rotating mirrors to correct positions in a switching matrix, when applying controlled voltages to Bubble or MEM switches (see Figure 6.11(a) and (b)), respectively.

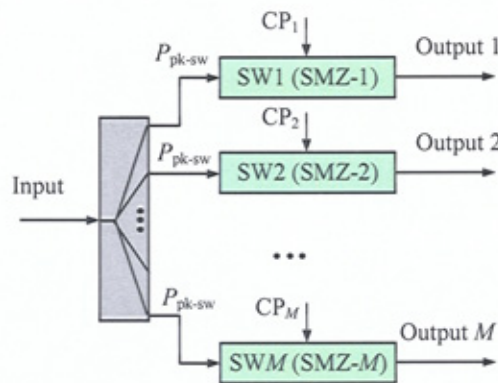


**Figure 6.11** (a) MEMS switch and (b) Bubbles switch

Unlike a large scale switch category, the ultrafast all-optical switches is constructed using individual  $1 \times 2$  SOA-based TOAD, UNI, SMZ and TaMZ (Section 2.4) offering

much faster responses in the order of few picoseconds and being optically controlled. However the main limitation of ultrafast optical switches is that the energy of a short (picoseconds-width) optical control pulse is insufficient to maintain the states of SOA nonlinear phase and gain changes over a long switching period of hundreds of picoseconds. Therefore ultrafast optical switches are typically used in optical processing and demultiplexing applications, where the required SW width is of the order of a few to tens of picoseconds.

The proposed PPM-HP router design is aimed at ultrafast routing, i.e. ultrafast header recognition and ultrafast-response switching of a long packet. Therefore SMZ switches are employed as the SWs in OSW for the router, with a dedicated optical CP to maintain a long ( $\sim$  nanoseconds) SW with a relatively constant gain property. Figure 6.12 shows a  $1 \times M$  OSW utilising  $M$  SMZs as the on/off switches controlled by  $CP_1, CP_2, \dots, CP_M$  with identical input packet power  $P_{pk-sw}$  (peak pulse power).



**Figure 6.12** A  $1 \times M$  OSW based on an array of  $M$  SMZ switches



The OSWC is used to generate  $CP_m$  for  $SMZ_m$  in the OSW ( $1 \leq m \leq M$ ).  $CP_m$  could be either (i) a constant power generated by the AOFF or (ii) a stream of high-powered multiple pulses. In the following sections, the AOFF and multiple-pulse generation are presented.

### 6.6.1 All-optical flip-flop

The all-optical flip-flop is an essential component for latching functions in high-speed all-optical processing and switching applications [22, 145, 206]. In this work, the AOFF is used to provide a constant-power long duration CP for the router OSW and for wavelength conversion in single and multiple wavelength routers, respectively. As a result, the switched packets, especially for a long packet, will receive an approximately constant gain. Currently, the AOFF can be realised by using the coupled/multimode-interference bi-stable laser diodes scheme [207-209], coupled SMZ [210] and a SMZ with a single-pulse counter-propagation control-signal feedback-loop [149]. In the former scheme, a number of wavelengths are required, whereas in the latter scheme only a single wavelength with a feedback-loop (FBL) is needed. Since there is a real time signal-propagation delay  $T_{FBL}$  associated with the FBL of hundreds of picoseconds (the waveguide length is about tens of millimetres) [149], a certain delay will be introduced into the feedback signal when switching AOFF to the ON state. Hence it requires a sufficient transient time equivalent to the  $T_{FBL}$  to set the AOFF output fully into an ON state. In addition in the proposed FBL scheme reported in [149], counter-propagation between a control and input signal in the SMZ will result in a slow AOFF response due to the counter-propagation effect in the SOA [156]. As a result, these proposed AOFFs

operate in the order of nanoseconds. Therefore in the FBL-based AOFF, achieving a fast response time and a narrow ON time (i.e. shorter than the transient time) is an issue. Here, a new AOFF configuration assisted by a feedback-loop SMZ with multiple forward control signals (set **S** and reset **R**) is proposed in this thesis to overcome these limitations.

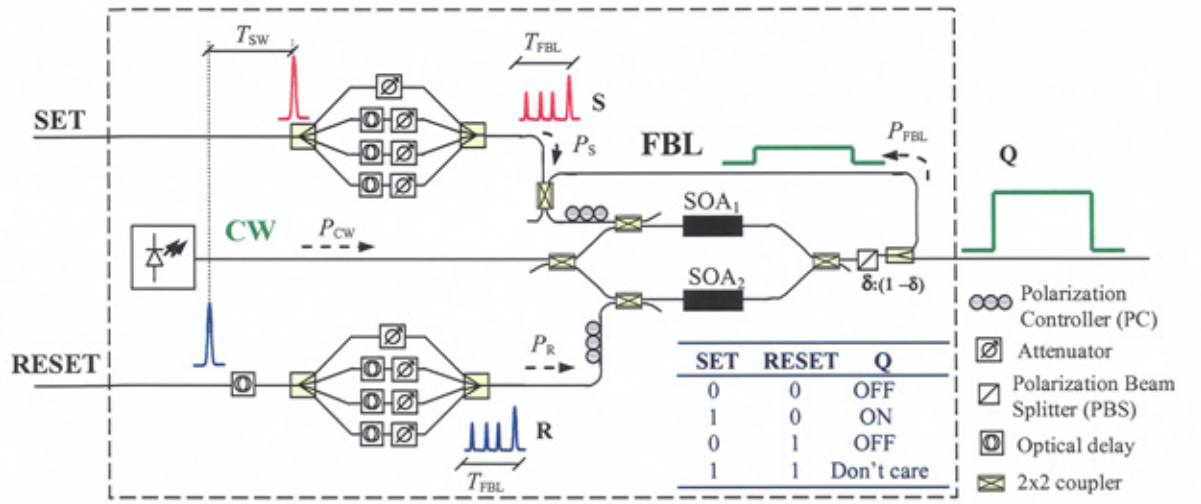


Figure 6.13 AOFF based on a single SMZ with the FBL and multiple forward Set/Reset signals

An AOFF circuit block diagram and its operation principle (truth-table) are depicted in Figure 6.13. The AOFF is composed of a SMZ switch with a continuous wave (CW) signal input, “set” and “reset” control pulses, and a FBL (with a signal propagation delay of  $T_{FBL}$ ) feeding  $\delta\%$  power from the AOFF output (**Q**) to the upper control arm of the SMZ. PCs are used to introduce an orthogonal-polarisation between the CW and CPs, and finally a PBS is used at the output of the SMZ to separate them. In the absence of the CPs, and provided both SOAs are identical, the SMZ is in a balanced state and the input CW signal will not emerge at the AOFF output (i.e. in OFF state). A single “set”

pulse passed through a number of paths with different delays and attenuators produces a multiplexed signal  $S$  within  $T_{FBL}$ .  $S$  is applied to the upper control input of the SMZ to toggle AOFF on (i.e. in ON state). The leading pulse of  $S$  saturates SOA<sub>1</sub> causing an imbalance in the gain and phase profiles between the two arms, thus switching the CW signal to the output  $Q$ . To keep the AOFF in the ON state, i.e. a flat SOA<sub>1</sub> gain saturation level, a portion  $\delta\%$  of the  $Q$  output power  $P_{FBL}$  is fed back to the upper control input of the SMZ. The feedback signal will take  $T_{FBL}$  time to arrive at the SOA<sub>1</sub>, therefore, until the arrival of  $P_{FBL}$ , the remaining pulses in  $S$  will ensure that the SOA<sub>1</sub> remains in saturation. This continuous saturation will preclude the SOA gain from recovering to its initial value when the first pulse exits SOA<sub>1</sub> whilst  $P_{FBL}$  is yet to arrive. Similar to the “set” pulse, a “reset” pulse, after a delay of packet duration  $T_{pk}$ , creates a multiple-pulse  $R$  applied to the lower control input of the SMZ. The first pulse of  $R$  saturates the SOA<sub>2</sub> gain, dropping it to the same level as the SOA<sub>1</sub> saturating gain (i.e. restoring the gain and phase balance between the SMZ arms). The gain balance will once again toggle AOFF to its OFF state, due to the CW no longer being switched to the output  $Q$ . Note that  $P_{FBL}$  is still in the upper control port, within a subsequent  $T_{FBL}$  period, with no output signal at  $Q$ . To retain the same gain level in both SOAs within this period, the remaining pulses in  $R$  will continue to saturate the gain of the SOA<sub>2</sub> until the SMZ is in the balanced state. Therefore the  $Q$  signal is completely turned-off during and after  $T_{FBL}$ , once the “reset” signal is applied.

#### 6.6.1.1 AOFF stability

To achieve operational stability, the feedback power should be the same as the average

powers of both the **S** and **R** signals. The feedback power will ensure steady imbalanced and balanced states in the SMZ during the transient durations when the AOFF is switched to ON and OFF states, respectively. These constraints are represented as follows:

$$P_{\text{FBL}} = \sum_{k=0}^{L_{\text{S}}-1} P_{\text{S,avg}} \left( t + \frac{kT_{\text{FBL}}}{L_{\text{S}}} \right), \quad (6.7)$$

$$\sum_{k=0}^{L_{\text{R}}-1} P_{\text{R,avg}} \left( t + \frac{kT_{\text{FBL}}}{L_{\text{R}}} \right) = \frac{P_{\text{FBL}}}{2}, \quad (6.8)$$

where  $P_{\text{S,avg}}(t)$  and  $P_{\text{R,avg}}(t)$  are the average powers of control pulses in the **S** and **R** streams, respectively, over  $T_{\text{FBL}}$ .  $L_{\text{S/R}}$  is the number of pulses in each **S** or **R**. In (6.7) when  $P_{\text{FBL}} < P_{\text{S,avg}}(t)$ , the output signal will eventually cease. On the other hand, a greater  $P_{\text{FBL}}$  will gradually saturate the SOA gain, thus saturating the AOFF-output gain. As a result, the output signal intensity fluctuates over a large range, which is determined by the intensity variation ratio (*IVR*) between the minimum and the maximum values of **Q** during  $T_{\text{pk}}$ . To turn the AOFF off completely,  $P_{\text{R,avg}}(t)$  should be equal to  $0.5 \times P_{\text{FBL}}$ , to ensure that both SOAs receive the same average control power (6.8). In the case where  $P_{\text{R,avg}}(t)$  is greater or smaller than  $0.5 \times P_{\text{FBL}}$ , a residual signal will emerge at the **Q** output, which in turn unexpectedly restores the AOFF to the ON state. The residual signal will therefore deteriorate the on/off contrast ratio at **Q**, which is defined by the power ratio of the signals in the ON and OFF states.

### 6.6.1.2 Characterisations

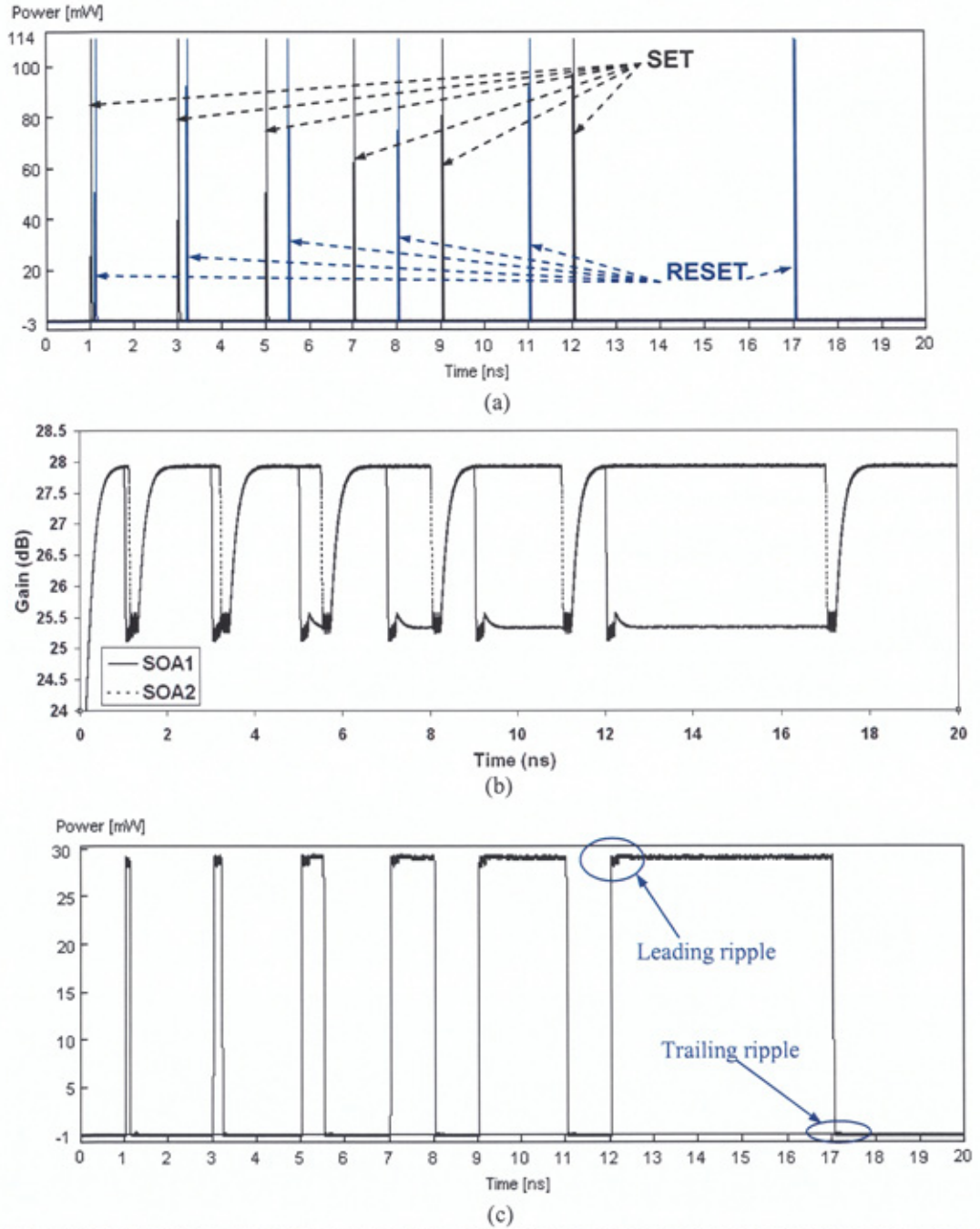
The AOFF operation, *IVR* and *CR* performance have been validated using the VPI simulation software. The AOFF simulation and SOA device parameters are given in Table 6.3 and Table 4.2.

**Table 6.3** AOFF parameters for operation and stability simulation

Parameters	Values
AOFF splitting factor - $\delta$	15%
AOFF input CW power - $P_{CW}$	0 dBm
AOFF feedback loop delay - $T_{FBL}$	0.2 ns
Set/Reset pulse width - FWHM	20 ps
Packet length - $T_{pk}$	0.1, 0.2, 0.5, 1, 2 ns
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
$P_S$ (peak power of first pulse)	13.5 dBm
$P_S$ (peak power of followed pulses)	8.5 dBm
$P_R$ (peak power of first pulse)	10.5 dBm
$P_R$ (peak power of followed pulses)	5.5 dBm
Number of pulses in <b>S</b> or <b>R</b>	4

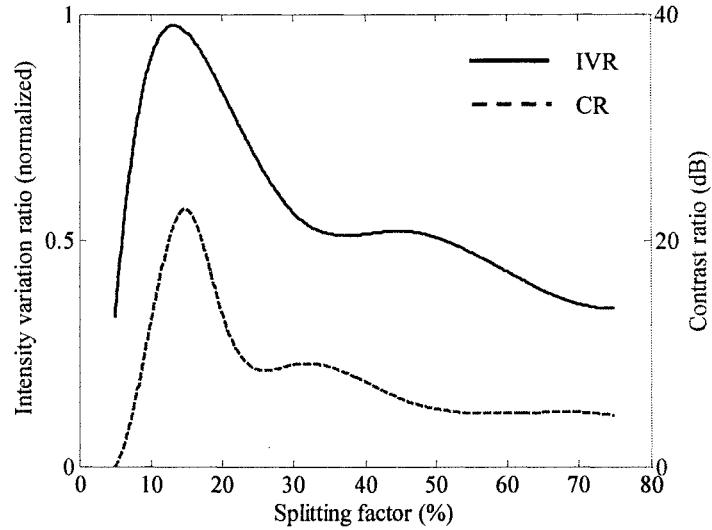
Note that  $P_{S,avg}(t)$  is 3 dB greater than  $P_{R,avg}(t)$ , to ensure that the SOAs are excited with same set/reset powers, since **S** is reduced by 3 dB when being coupled with  $P_{FBL}$ .  $T_{FBL}$  is selected to be 0.2 ns, approximately equivalent to a 40-mm optical waveguide FBL [149]. The operation of the flip-flop is illustrated in Figure 6.14. “Set” and “reset” pulse trains, shown in Figure 6.14(a), are applied to the AOFF over a range of different  $T_{pk}$  values: 0.1, 0.2, 0.5, 1, 2 and 5 ns. The resultant temporal gain profiles of the SOAs, corresponding with set/reset signals, are monitored as shown in Figure 6.14(b). During

an ON period of  $T_{pk}$  the gain of SOA<sub>1</sub> is kept at a constant saturated level when either being excited by S or the delayed  $P_{FBL}$ .



**Figure 6.14** Illustration of AOFF operation (a) AOFF input Set/Reset pulses, (b) temporal gain profiles of SOA<sub>1</sub> and SOA<sub>2</sub> and (c) AOFF output (Q)

Figure 6.14(c) displays the AOFF output waveforms where there is a small amount of ripples at the leading edge signal (i.e. ON state during  $T_{FBL}$  period), owing to the variation in the  $SOA_1$  gain profile caused by the discrete excitations of pulses in **S**. When the AOFF is switched off, a small residual signal (trailing ripples) lasting  $T_{FBL}$ , still emerges at **Q**, thus resulting in on/off *CR* deterioration. This is due to the difference between the gain variation in  $SOA_2$  caused by multiple-pulse excitations from **R**, and the flat gain profile of the  $SOA_1$  maintained by a left-over of the constant  $P_{FBL}$  within that  $T_{FBL}$ .



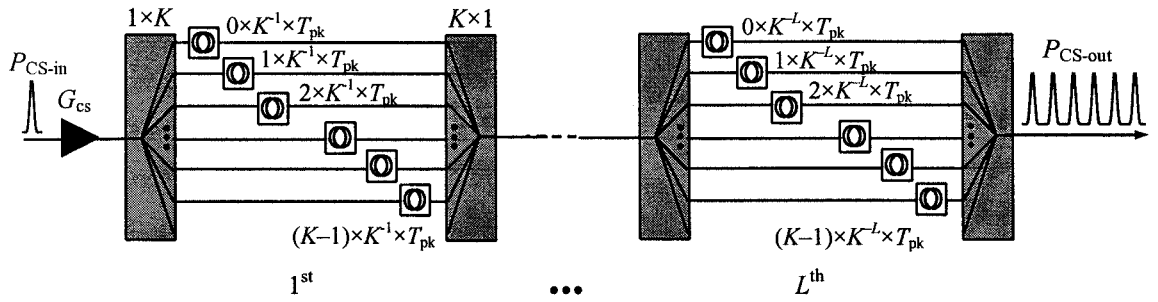
**Figure 6.15** The AOFF's intensity variation ratio *IVR* and contrast ratio *CR* performance against the splitter factor  $\delta$

The graphs in Figure 6.15 show the *IVR* and *CR* performance of the proposed AOFF against the splitting factor  $\delta$ . Figure 6.15 shows that the highest value of *CR* is 22 dB for  $\delta = 15\%$  and  $T_{pk} = 1\text{ns}$  (AOFF total output power is 28 mW (14.5 dBm)). It is also

shown that the AOFF output signal is relatively flat during  $T_{pk}$  as  $IVR$  is 0.95 when  $\delta = 15\%$ . Beyond the optimum operation point ( $\delta = 15\%$ ), both  $CR$  and  $IVR$  are considerably reduced due to high residual power and inappropriate feedback power, respectively.

### 6.6.2 Multiple-pulse generation

A multiple-pulse generation circuit, including a  $L$ -stage chain of  $K$  delay units to generate the optical pulse stream, is depicted in Figure 6.16.



**Figure 6.16** A  $L$ -stage chain of  $K$  delay units for generating a multiple-pulse stream of control signal

Each delay stage  $l$  ( $1 \leq l \leq L$ ) contains  $K$  delay units and each unit in the  $l^{\text{th}}$  stage has a delay step difference of  $K^{-l} \times T_{pk}$ . Therefore the CP stream will contain  $K^L$  pulses with the temporal interval of  $K^{-L} \times T_{pk}$ . Typically this interval is set to be smaller than the SOA recovery gain to ensure the reduction of the small router's switching gain fluctuation.



Assuming that the excess loss for the  $1 \times K$  splitter and  $K \times 1$  combiner is the same as  $L_{\text{excess}}$ , the target peak power of the CP stream is  $P_{\text{CS-out}}$  and the preamplifier gain is  $G_{\text{CS}}$ , the minimum power of the input pulse  $P_{\text{CS-in}}$  is required as:

$$P_{\text{CS-in}} (\text{dB}) = 10 \log_{10} (P_{\text{CS-out}}) - G_{\text{CS}} + L \times 10 \log_{10} (K) + L_{\text{excess}}. \quad (6.9)$$

The multiple-pulse stream generator could be also used for PPM-HEM with the stream duration of  $T_{\text{CP-HEM}}$  (instead of  $T_{\text{pk}}$ ).

### 6.6.3 Noise and crosstalk in optical switch

The ultrafast optical switch introduces noise and crosstalk on the switched signal which corrupts the switched data signal, i.e. deteriorating the received optical signal-to-noise ratio (OSNR), especially in a multiple-hop routing. The noise associated with the switch originates from the SOA ASE noise. Assuming that the switch gain is maintained at a constant value  $G_{\text{OSW}}$  by using either a pulse stream or an AOFF controlling scheme, the unpolarised ASE noise power is given by [5, 191]:

$$P_{\text{ASE}} = 2n_{\text{sp}} h f_0 (G_{\text{OSW}} - 1) B_0, \quad (6.10)$$

where  $h f_0$  and  $B_0$  are the product of Planck constant with the operating optical frequency (photon energy) and the optical bandwidth of the system (i.e. the optical filter bandwidth), respectively.  $n_{\text{sp}}$  is the optical amplifier inversion parameter and its relation to the switch noise figure  $NF_{\text{OSW}}$  is expressed by [1]

$$n_{\text{sp}} = \frac{NF_{\text{OSW}} G_{\text{OSW}}}{2(G_{\text{OSW}} - 1)}. \quad (6.11)$$

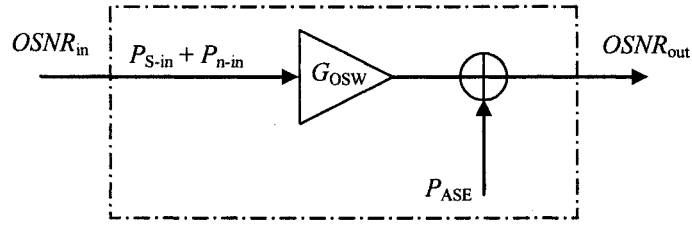
Assuming that the OSNR of the input signal ( $OSNR_{in}$ ) is given by

$$OSNR_{in} = \frac{P_{S-in}}{P_{n-in}} \quad (6.12)$$

The deteriorated OSNR at the output signal ( $OSNR_{out}$ ) is therefore computed as

$$OSNR_{out} = \frac{G_{OSW} \times P_{S-in}}{G_{OSW} \times P_{n-in} + P_{ASE}} \quad (6.13)$$

The switch noise and OSNR expressed in (6.10) and (6.13) are depicted in the ASE noise modelling diagram in Figure 6.17.



**Figure 6.17** ASE noise modelling in OSW

Switching crosstalk ( $CXT$ ) could be due to (i)  $RCXT$  from the residual signal power following the switched packet due to imperfect closure of the switching window (Section 4.2) and (ii) the power leak from the control signal to the switched signal due to incomplete separation between the data and signal at the switch output, i.e. data-control crosstalk ( $CXT_{D-CP}$ ) [130]. To minimise the  $RCXT$ , an empty (no signal) guard band (comparable to the SOA gain recovery time) is placed between successive packets to ensure the optical switch gain is fully recovered before the arrival of the next packet.

Typically the control and data signals will have different wavelengths, be orthogonally polarised, or be injected in opposite directions so that they are easily identified and can be separated at the output of the SMZ. However, a certain amount of power from the CP could still be with the data signal due to the optical filter low resolution, imperfect polarisation beam splitter and the XGM, respectively. This will lead to  $CXT_{D-CP}$  which is a subject investigated in Chapter 7.

## 6.7 Summary

The chapter has presented the architectures and characterisation of all of the modules employed in the proposed PPM-HP router. Self clock extraction, based on two inline SMZs was proposed, offering a high on/off contrast ratio ( $\sim 20$  dB). In addition the inline SMZ structure requires no feedback loop, resulting in operation stability for the clock recovery process. The PPM header extraction module includes the serial-to-parallel converter, and the PPM address conversion module was presented. A high contrast ratio ( $> 20$  dB)  $1 \times 2$  switch, based on a pair of SMZs, was proposed for the implementation of a chain of  $N$   $1 \times 2$  switching stages, in order for correct conversion of the PPM address. A PPRT was constructed using an array of passive delay units for both small and medium size networks ( $N = 4$  to 8 bits). A single-bitwise correlation between the converted PPM address and the PPRT entries was implemented using optical AND gates based on the SMZ. The effect of timing offset between two AND inputs was examined. Finally, OSW, with the assistance of either a AOFF or multiple-pulse generator, was presented. The proposed AOFF using forwarded multiple-pulse controls offers a fast response and overcomes the delay associated with the feedback loop. Noise

and crosstalk associated with the optical switch were determined, in order to study router performance in Chapter 7.

The findings in this chapter were published as follows: papers [A4] and [A16] presented the CEM principle and characterised its performance. Results and discussions of PPM-ACM including SPC and HEM were described in [A11], [A15], [A18], [A21] (for header addresses with  $N = 8$  bits) and [A22]. PPRTs and AND gates were mentioned in [A11], [A12], [A14], [A19], [A21] and [A22]. The all-optical flip-flop was introduced and investigated in [A3], [A10], [A12] and [A14]. SMZ-based optical switches and the associated noises were investigated in [A4], [A5] and [A11].

## **CHAPTER 7**

# **ROUTER SIMULATIONS AND PERFORMANCE INVESTIGATIONS**

### **7.1 Introduction**

In Chapters 5 and 6 the principle of PPM-HP router architecture and its main elements including their characterisations were discussed. In this chapter, the router operation and its performance are investigated theoretically and by means of VPI simulation. Chapter 7 begins with the simulation of the proposed single and multiple-wavelength routers using VPI simulation software. Investigation of the router performance will focus on (i) the reliability of packet header recognition and (ii) multiple-hop routing performances including accumulated crosstalk and optical signal-to-noise-ratio. Finally, the router features and specifications are presented.

## 7.2 Simulations of Single and Multi-Wavelength (WDM) Routers

### 7.2.1 Single-wavelength router

The block diagram of the three-hop routing optical system ( $H = 3$ ) based on the VPI simulation is shown in Figure 7.1. It consists of a source node, three  $1 \times 3$  PPM-HP based routers, an optical pre-amplifier, standard single mode fibres (SSMF), dispersion compensation fibres (DCF), attenuators and a target node (assumed with the address #8). Data packets generated at the source node are amplified and passed through a number of routers and optical fibre links before arriving to the target node. Attenuators are used to maintain at a constant packet power at each router input. The configurations of PPRTs for three routers (i.e. three core nodes) are given in Table 7.1.

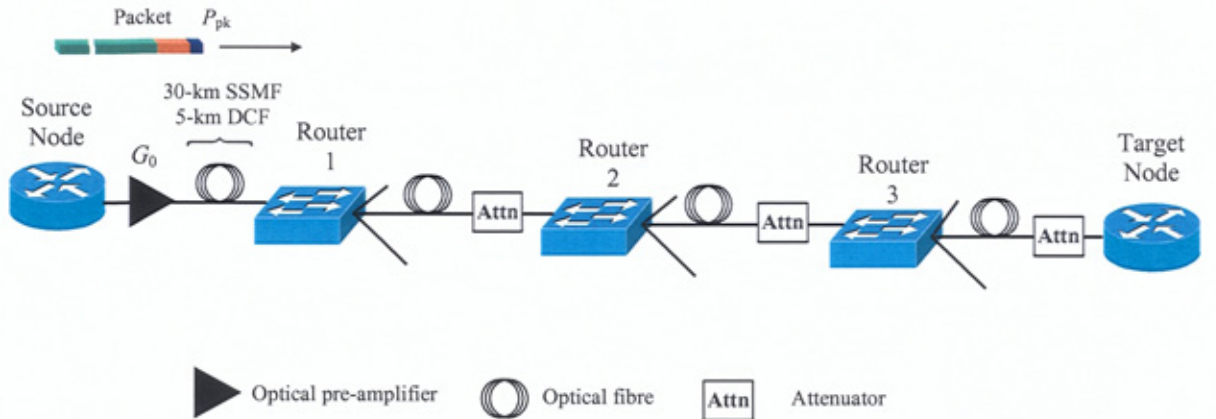
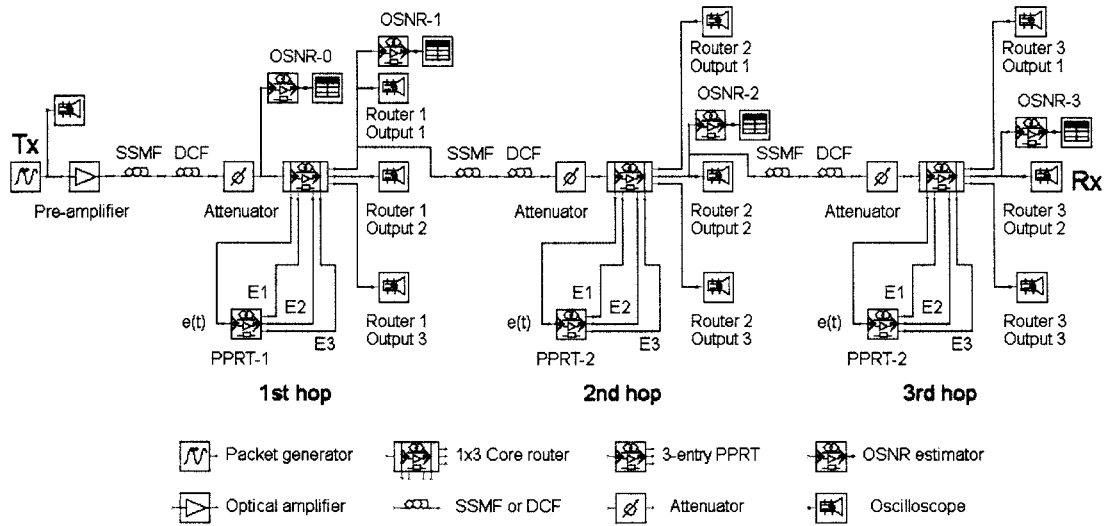


Figure 7.1 Three-hop routing optical system based on PPM-HP

**Table 7.1** PPRTs of three intermediate routers (for  $N = 4$ ,  $M = 3$ )

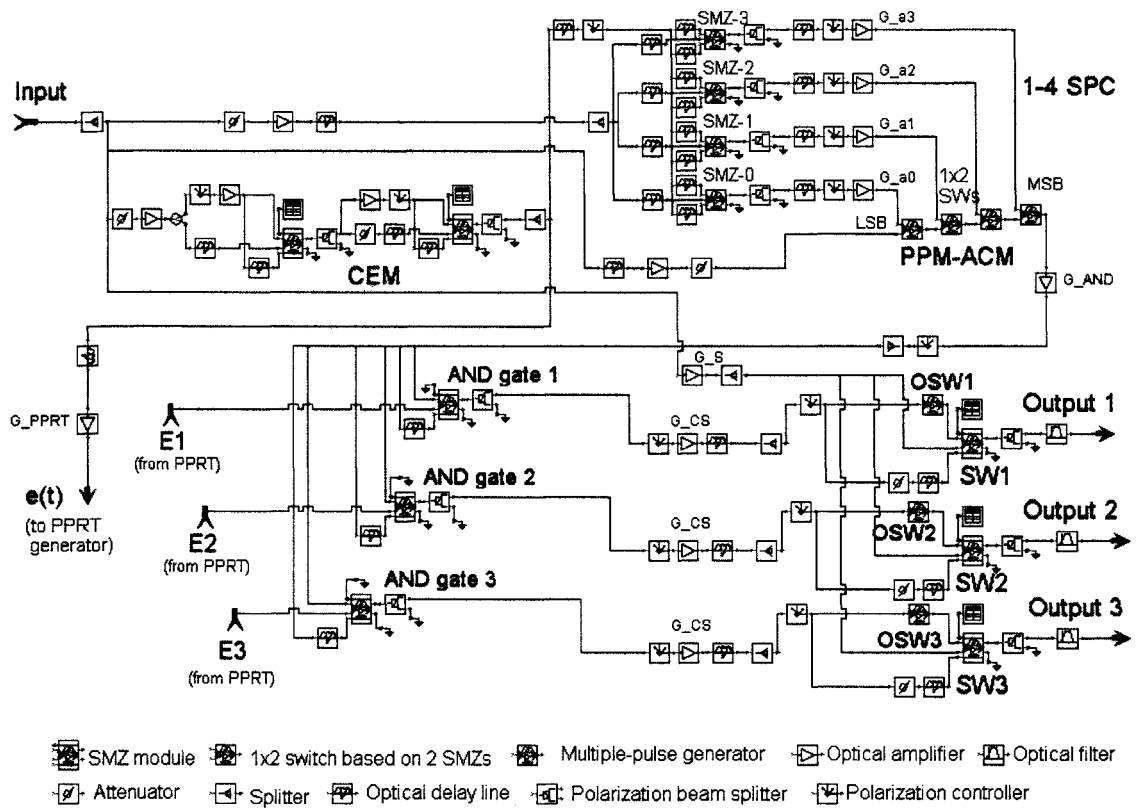
PPRT entries	Equivalent router outputs	Output sets	Core router 1	Core router 2	Core router 3
$E_1$	$OP_1$	$D_1$	0,1,2,5,8,12,14	1,2,3,9,10	4,6,7,12,13
$E_2$	$OP_2$	$D_2$	0,3,7,10,13,15	4,8,12,14,15	0,3,8,11,15
$E_3$	$OP_3$	$D_3$	0,1,4,6,9,11	0,5,6,7,11,13	1,2,5,9,10,14

The simulation schematic diagrams of the optical system, the PPM-HP router and 3-entry PPRT-1 are depicted in Figure 7.2, Figure 7.3(a) and (b), respectively.

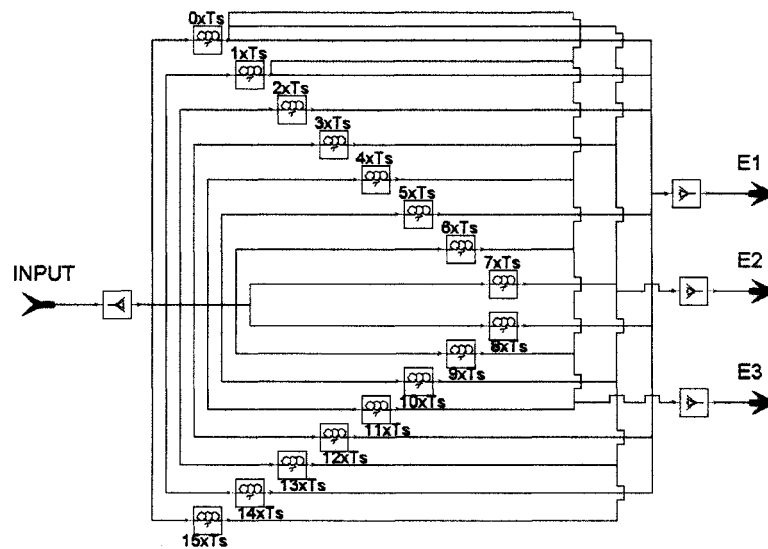


**Figure 7.2** VPI schematic diagram of multiple-hop routing based on PPM-HP

Figure 7.3(a) and (b) show schematic diagrams of a  $1 \times 3$  PPM-HP router (including the CEM, SPC, PPM-ACM, AND gates, OSWC and OSW) and the 3-entry PPRT-1. Simulation parameters are given in Table 7.2 and Table 4.2.



(a)



(b)

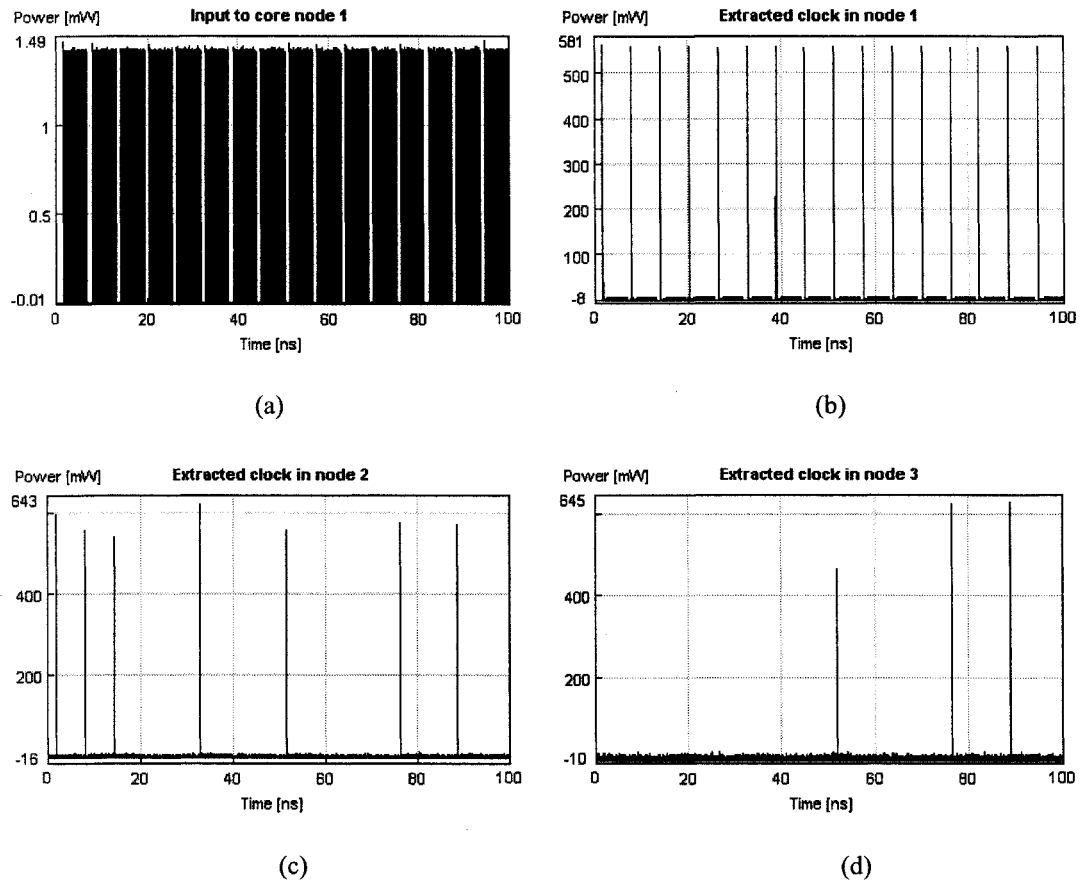
Figure 7.3 VPI schematic diagram of (a) 1x3 PPM-HP router and (b) 3-entry PPRT-1 circuit diagram



**Table 7.2** Simulation parameters for three-hop routing based on single-wavelength PPM-HP router

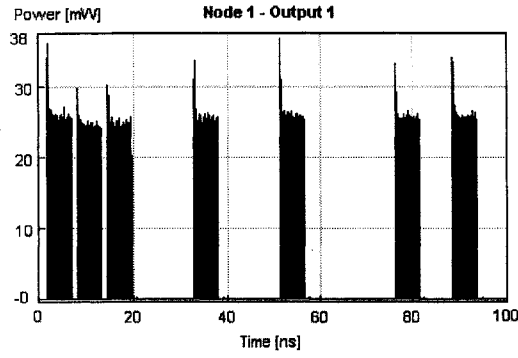
Parameters	Values
Input data bit rate	100 Gbit/s
Data packet length	64 bytes (512 bits)
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Data & CP width - FWHM	2 ps
PPM slot duration - $T_s$	5 ps
Number of address bits - $N$	4
Number of router output - $M$	3
SSMF length	30 km
DCF length	5 km
Preamplifier noise figure - $NF_0$ (Preamplifier inversion parameter - $n_{sp}$ )	4.5 dB (1.4)
Data pulse (peak) power - $P_{pk}$	1.45 dBm (1.4 mW)
Input splitting factor - $\kappa$	0.25
Packet duration - $T_{pk}$	5.17 ns
Optical bandwidth - $B_0$	300 GHz
$G_h$ ( $h = 1, 2, \dots, H$ )	18 dB
Total loss of a hop - $L_h$ ( $h = 1, 2, \dots, H$ )	- 18 dB
Pre-amplifier gain - $G_0$	9 dB
First span loss - $L_0$	- 9 dB
CEM switching window width - $T_{sw}$ (CEM)	6 ps
CEM SMZ-1 amplifier gain - $G_{CP}$	9 dB
CEM SMZ-2 attenuation - $\alpha$	12 dB
PPRT coupler/splitter excess loss - $L_{excess}$	1 dB
PPRT entry pulse peak power - $P_{E-m}$	0 dBm (1 mW)
SPC switching window width - $T_{sw}$ (SPC)	5 ps
Number of CPs for PPM-HEM ( $K^L$ )	4 ( $K = 4, L = 1$ )
AND switching window width - $T_{sw}$ (AND)	5 ps
OSW packet input (peak) power - $P_{pk-sw}$	- 3 dBm (0.5 mW)
OSW CP peak power - $CP_m$	5 mW
Number of CPs for OSW ( $K^L$ )	64 ( $K = L = 4$ )
OSW noise figure - $NF_{OSW}$	6 dB

The transmitted packet comprises of a single clock bit, a 4-bit header address and a 512-bit payload. Sixteen optical data packets, having target addresses indexed from 0 to 15, are transmitted at 100 Gbit/s from the source node with 1 ns packet guard band, see Figure 7.4(a). The extracted clock pulses from the incoming packets observed at the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> core routers are displayed in Figure 7.4(b), (c), and (d), respectively.

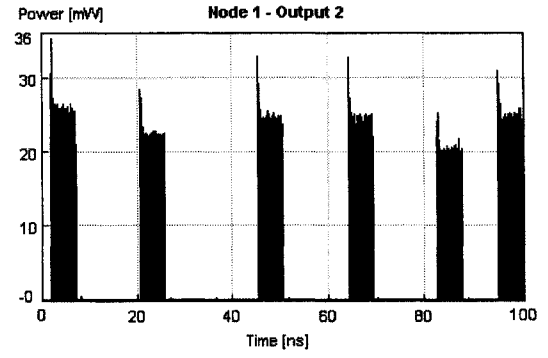


**Figure 7.4** The time waveforms: (a) input packets, the extracted clock at (b) router (node) 1, (c) at router 2, and (d) at router 3

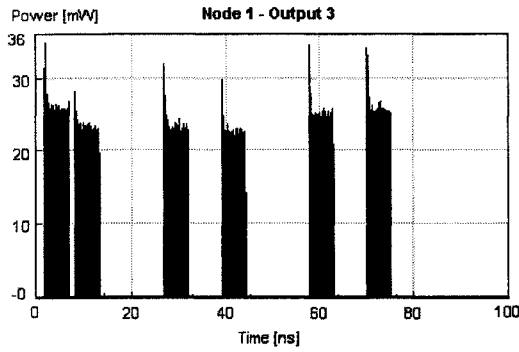
In the first hop, input packets are switched to the router outputs OP<sub>1</sub>, OP<sub>2</sub> and OP<sub>3</sub>, see Figure 7.5(a), (b) and (c), corresponding to the PPRT of router 1 given in Table 7.1.



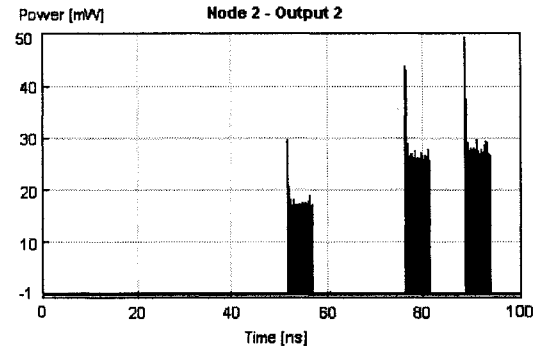
(a)



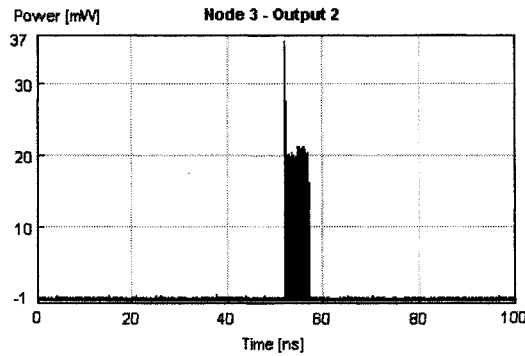
(b)



(c)



(d)



(e)

**Figure 7.5** The time waveforms of switched packets to the (a) router 1 - output 1, (b) router 1 - output 2, (c) router 1 - output 3, (d) router 2 - output 2, (e) router 3 - output 2

At the 2<sup>nd</sup> and the 3<sup>rd</sup> hops, packets with the target address #8 arriving to routers 2 and 3 are switched to OP<sub>2</sub> of router 2 and also OP<sub>2</sub> at router 3, see Figure 7.5(d) and (e),

respectively. Finally, a packet reaches the intended target node #8 after being routed via 3 core routers.

Note from Figure 7.5(a) - (e) power overshooting is present at the start of the switched packets. The overshooting is due to the pulses at the start of the switched packet receiving a high OSW gain which in turn gradually saturates the OSW gain, thus the subsequent pulses in the switched packet will receive a lower switching gain. The overshooting also depends on the number of bits “0”s and “1”s at the start of incoming packets, accumulating as packets propagate through the multiple routers. This effect could be seen intuitively from the magnitude variation of the extracted clock pulses and hence switched packets with different bit patterns at different routers’ outputs. Figure 7.4 and Figure 7.5 show the magnitude variation of the extracted clock and switched packets after multiple hops. This is due to the clock pulse intensities being further increased (by the overshooting effect) after each hop.

Note that the PPRT of core router 1 in Table 7.1 defines the broadcasting and multicasting transmission modes for the incoming packets with target addresses of #0 and #1. As a result, router 1 will switch packets with an address of #0 to all outputs, and packets with address of #1 only to outputs 1 and 3. This transmission-mode selection property of the PPM-HP router allows the grouping of a number of different target nodes using the same address such as #0 or #1.

### 7.2.2 WDM PPM-HP router operation

A 1×3 WDM PPM-HP router simulation model is based on the router architecture described in Figure 5.5. The input signal includes nine packets with three different wavelengths  $\lambda_1$ ,  $\lambda_2$  and  $\lambda_3$  (three packets per wavelength). Each packet contains a clock bit, a 4-bit address and a payload. The packet header addresses (in decimal values) are listed in Table 7.3 where the number  $m$  in brackets indicates that the packet will be switched to the  $m^{\text{th}}$  router output with the routing information given in the MW-PPRT shown in Figure 5.6(b).

**Table 7.3** Target addresses for the incoming packets input in the multiple wavelength PPM-HP router

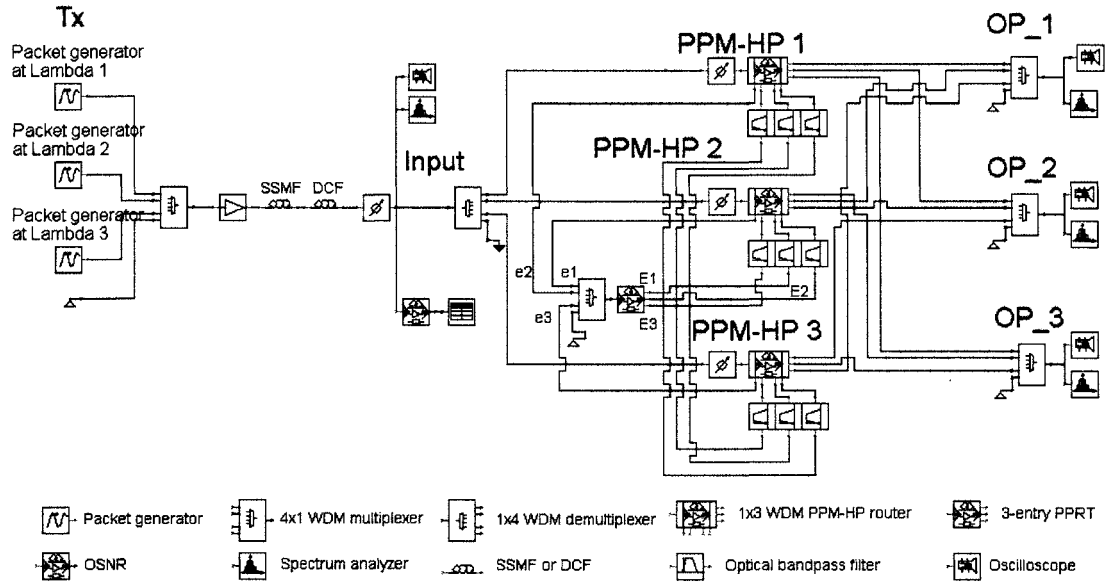
<b>Wavelengths</b>	Decimal address in packet 1 Address ( <i>Output</i> )	Decimal address in packet 2 Address ( <i>Output</i> )	Decimal address in packet 3 Address ( <i>Output</i> )
$\lambda_1$	4 (3)	7 (2)	13 (2)
$\lambda_2$	9 (3)	3 (2)	1 (1 and 3)
$\lambda_3$	15 (2)	4 (3)	5 (1)

The main simulation parameters used are given in Table 7.4 and the SOA parameters were given in Table 4.2. The parameters of PPM-HP module were adopted from Table 7.2.

**Table 7.4** Simulation parameters for single-hop routing based on multiple-wavelength PPM-HP router

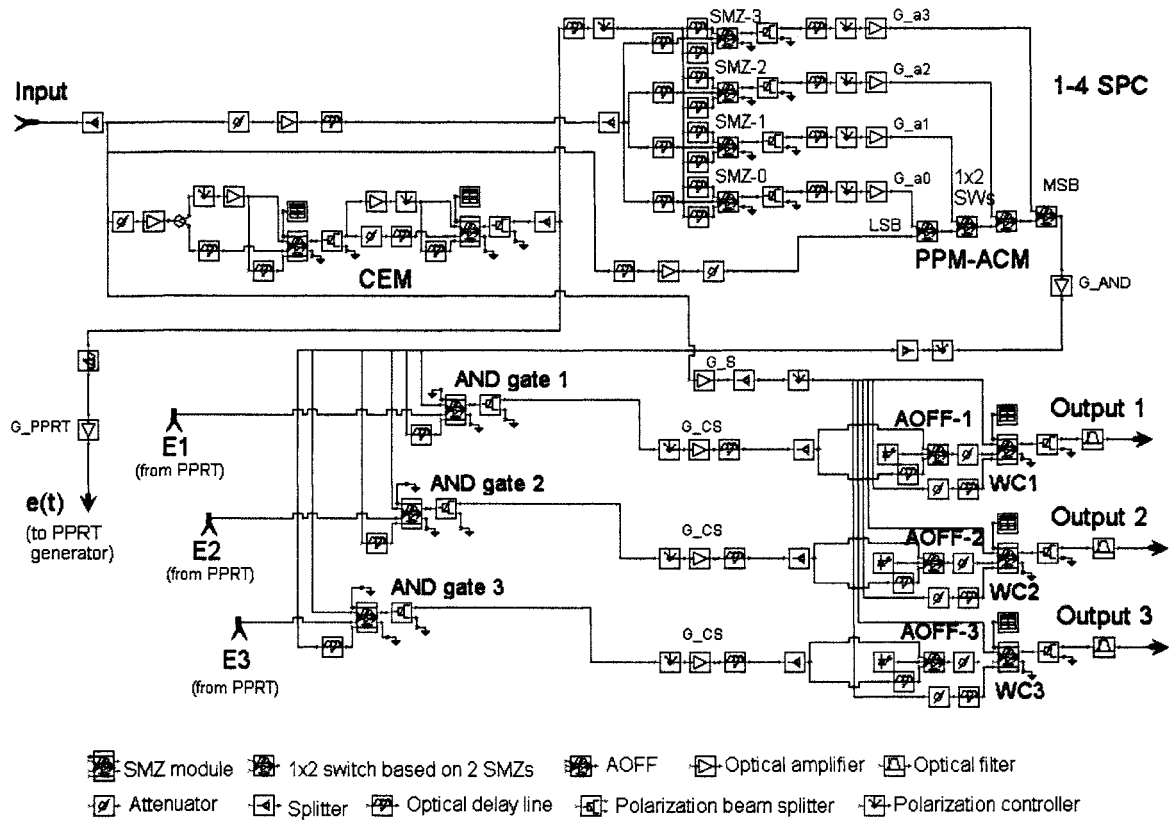
Parameters	Values
Input data bit rate	100 Gbit/s
Data packet length	16 bytes (128 bits)
Bit duration - $T_b$	10 ps
Data & CP width - FWHM	2 ps
PPM slot duration - $T_s$	5 ps
Data pulse (peak) power (each wavelength)	1.45 dBm (1.4 mW)
Number of address bits - $N$	4
Number of router output - $M$	3
Optical wavelength - $\lambda_1$ (equivalent to optical frequency - $f_1$ )	1569.8 nm (191.1 THz)
Optical wavelength - $\lambda_2$ (equivalent to optical frequency - $f_2$ )	1561.7 nm (192.1 THz)
Optical wavelength - $\lambda_3$ (equivalent to optical frequency - $f_3$ )	1553.6 nm (193.1 THz)
Optical bandwidth - $B_o$	300 GHz
AOFF input CW power - $P_{CW}$	3 dBm (2 mW)
AOFF feedback loop delay - $T_{FBL}$	0.1 ns
AOFF splitting factor - $\delta$	12.5%

Figure 7.6 shows a schematic diagram of the simulation setup for the proposed 1×3 WDM router. It mainly consists of a WDM transmitter (transmitting streams of optical packets at  $\lambda_1 = 1569.8$  nm,  $\lambda_2 = 1561.7$  nm and  $\lambda_3 = 1553.6$  nm), fibre span and the proposed 1×3 router with three PPM-HP modules. Packets at different wavelengths  $\lambda_1$ ,  $\lambda_2$  and  $\lambda_3$  arriving at the router input are first demultiplexed and processed in PPM-HP modules 1, 2 and 3, respectively. The outputs of the PPM-HP modules are multiplexed before emerging from the router outputs 1, 2 and 3. PPRT entries  $E_1$ ,  $E_2$  and  $E_3$  are generated by passing  $e_i$  ( $i = 1, 2$  and  $3$ ) through the delay lines within the 3-entry PPRT, see example in Figure 7.3(b).



**Figure 7.6** VPI schematic diagram of a 1×3 WDM PPM-HP router

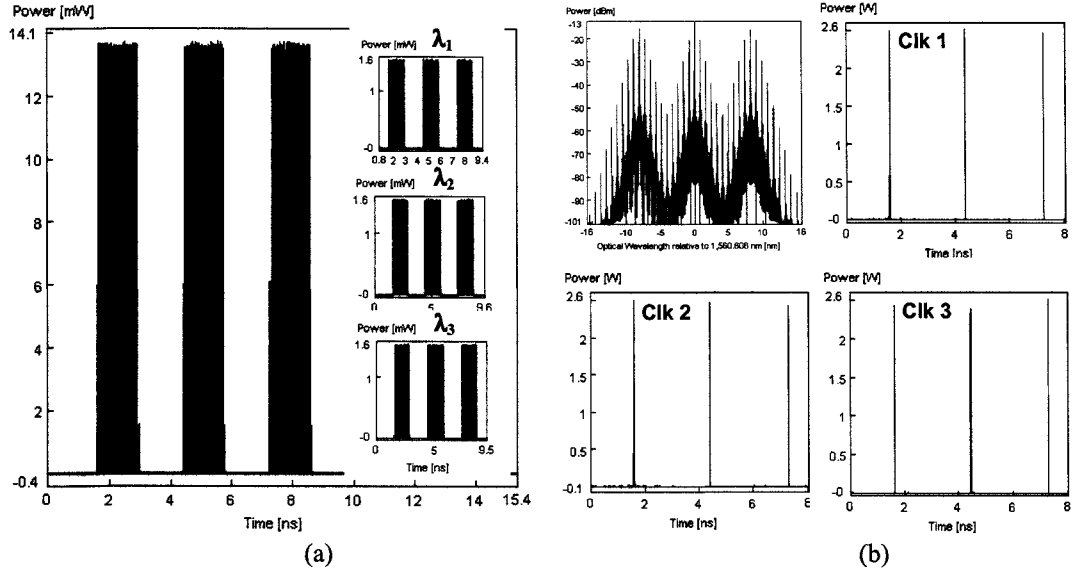
The sub-schematic (galaxy) for PPM-HP module is shown in Figure 7.7 including the CEM with two cascading SMZ switches, a 1-4 SPC employing SMZs, PPM-ACM, an array of three optical AND gates and three SMZ-based wavelength conversion (WC) modules incorporated with the AOFFs operating at  $\lambda_1$ ,  $\lambda_2$  and  $\lambda_3$  [157].



**Figure 7.7** VPI schematic diagram of a 1×3 PPM-HP router at individual wavelength employing AOFFs and WCs

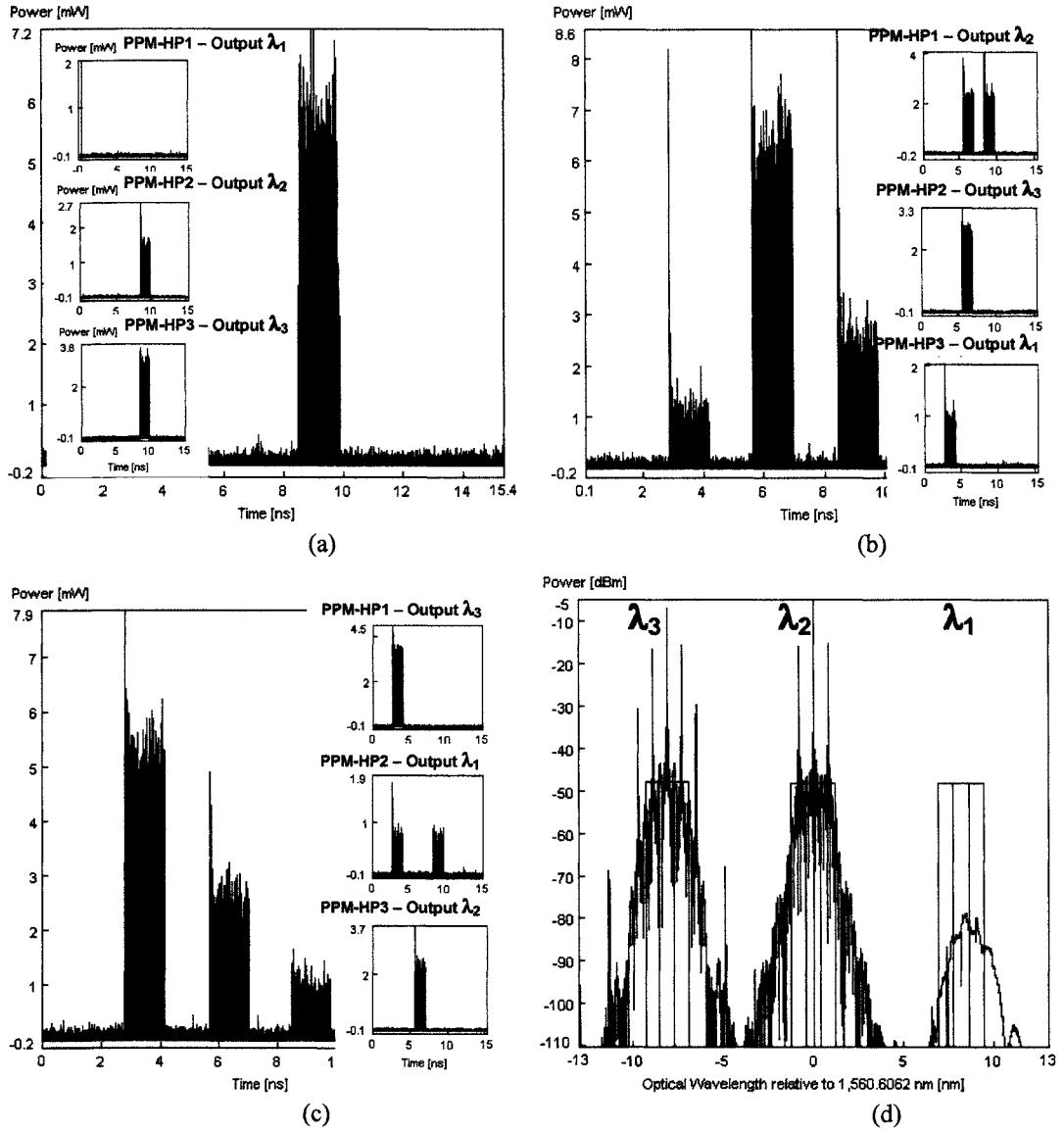
Figure 7.8 shows the temporal waveform and the corresponding power spectra at the router input and extracted clocks at three PPM-HP modules for MW PPM-HP. The input packet waveforms are given in Figure 7.8(a) where the insets illustrate the pre-multiplexed individual packets at three different wavelengths. The input packet optical power spectrum and the extracted clock pulses in the PPM-HP<sub>1&2&3</sub> modules are depicted in Figure 7.8(b).





**Figure 7.8** (a) Input packets applied to the router, insets: packets at separate wavelengths, (b) input signal spectrum (top-left) and extracted clock pulses at PPM-HP<sub>1&2&3</sub>

The signal waveforms presented in Figure 7.9(a), (b) and (c) corresponding to the multiplexed (switched) signals at the router outputs 1, 2 and 3, respectively. The intensity differences in these signals are due to the overlapping of switched packets from all PPM-HP modules being multiplexed at the router output. The insets in Figure 7.9(a), (b) and (c) show the converted packets to different wavelengths after PPM-HP modules which are combined at the router outputs 1, 2 and 3, respectively. The overshooting seen at the start of the switched packets is due to the transient gain process associated with the rapid changes in the SOA carrier density in the SMZ used for WC. The multicast transmission mode for packets with the address #1 (in decimal) is demonstrated as the switched packets emerging at both outputs 1 and 3 of the router. This can be seen from Figure 7.9(a) and (c) where the input packet to PPM-HP 2 is wavelength-converted into two packets at  $\lambda_2$  and  $\lambda_1$  emerging at PPM-HP 2 outputs, respectively.



**Figure 7.9** Signal waveforms at (a) router output 1, insets: packets to output 1 before being multiplexed, (b) router output 2, insets: packets to output 2 before being multiplexed, (c) router output 3, insets: packets to output 3 before being multiplexed and (d) power spectrum at the router output 1

The power spectrum at router output 1 showing the two main wavelengths,  $\lambda_2$  (from PPM-HP 2) and  $\lambda_3$  (from PPM-HP 3), is displayed in Figure 7.9(d). Also shown is the

noise level presented as bars. From the graph, the observed OSNR is better than the required 20 dB (the standard OSNR for an optical transmission system [5]). Further analysis and simulation of the OSNR will be presented in the next section.

### 7.3 PPM-HP Performance

The PPM-HP is the key part of the router in making the decision for switching an incoming packet to an intended router output. Its performance is affected by the presence of:

- Multiple pulses at the PPM-HEM output. Unwanted pulses along with the PPM-address in  $a_{\text{PPM}}(t)$  will lead to a wrong matching outcome in (5.4).
- The timing offset between the PPM-address pulse in  $a_{\text{PPM}}(t)$  with an PPRT entries. The timing offset will affect the resultant matching pulse intensities.

These effects will lead to the incoming packet being incorrectly switched to a wrong router output(s).

#### 7.3.1 Multiple-pulse effect in PPM-HEM

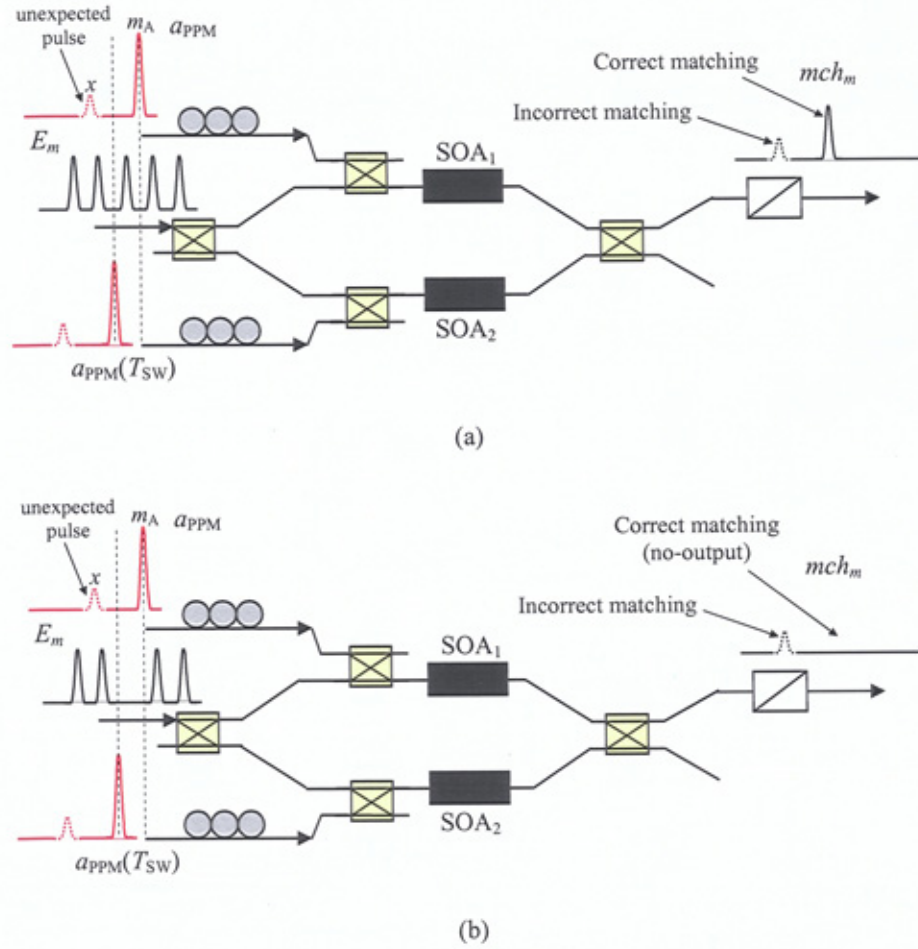
Due to non-zero inter-output contrast ratio in the switching stages of the PPM-HEM, there are up to  $2^N - 1$  unwanted pulses along with the PPM-address in  $a_{\text{PPM}}(t)$ . However, assuming that the PPM-HEM consists of  $N$  1×2 switching stages with unity net gain and an inter-output contrast ratio  $CR_{\text{OP12}}$  the maximum intensity of these pulses only

depends on the unwanted pulse intensity at the last output stage. This is due to other unwanted pulses at the input of the last stage having lower intensities than the  $CP_{\text{PPM-ACM}}$  intensity pulse. The maximum intensity of undesired pulses is computed by:

$$P_{\text{PPM-HEM,max}} = \frac{P_{CP_{\text{PPM-ACM}}}}{CR_{\text{OP12}}}. \quad (7.1)$$

where  $P_{CP_{\text{PPM-ACM}}}$  is the power of the PPM-address (i.e.  $CP_{\text{PPM-ACM}}(t + m_A \times T_s)$  in equation (5.2)) of  $a_{\text{PPM}}(t)$ . The amplified  $a_{\text{PPM}}(t)$  is used to enable the SMZ-based AND gates, see Figure 7.3(a). Assuming that the amplified  $P_{\text{PPM-HEM,max}}$  (located at position  $x$  in  $a_{\text{PPM}}(t)$ ) is applied to an AND gate where its input has a PPRT  $m$  entry having a pulse at the location  $x$ , the matching pulse  $mch_m$  will be non-zero at the location  $x$ , as shown in Figure 7.10(a) and (b). There will be two cases:

- If  $mch_m$  contains pulses at both positions  $x$  and  $m_A$ , see Figure 7.10(a), the router still switches the packet to its desired output  $m$ .
- If  $mch_m$  contains only a single pulse at position  $x$ , see Figure 7.10(b), the router switches the packet to its undesired output  $m$  (i.e. incorrect operation of PPM-HP).

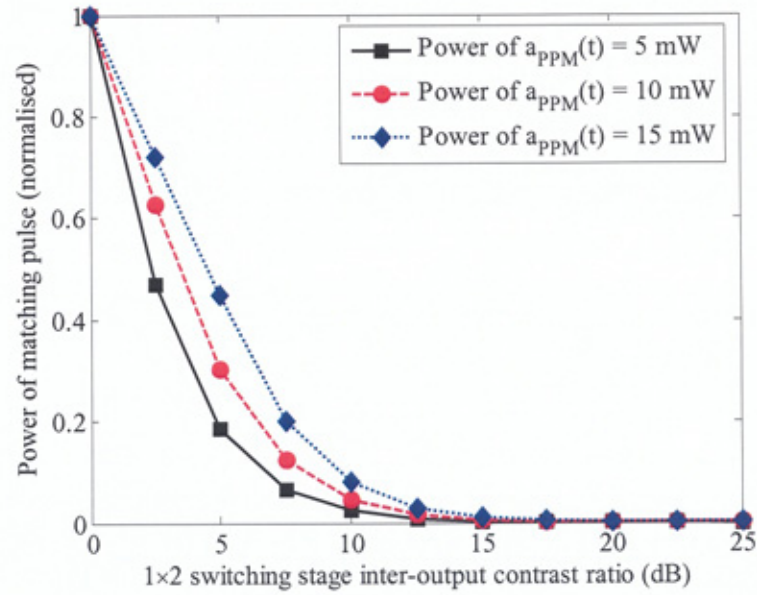


**Figure 7.10** Multiple-pulse effect in  $a_{PPM}$  results in (a) incorrect matching pulse and routing decision and (b) incorrect matching pulse but correct routing decision

Figure 7.11 shows the simulated matching pulse intensity (normalised) against the last switching stage inter-output contrast ratio  $CR_{OP12}$  for a range of different  $a_{PPM}$  powers to evaluate the  $mch_m$  in case of incorrect operation of PPM-HP, see Figure 7.10(b). Simulation and SOA parameters are given in Table 7.5 and Table 4.2, respectively.

**Table 7.5** PPM-HEM parameters for multiple-pulse effect calculation

Parameters	Values
Number of packet header address bits - $N$	4
Power of $a_{PPM}$	7 dBm, 10 dBm and 11.7 dBm (5 mW, 10 mW and 15 mW)
Power of PPRT entry - $P_{E-m}$	0 dBm (1 mW)
$P_{CP_{PPM-ACM}}$	0 dBm (1 mW)
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Net gain of each switching stage	0 dB
PPM slot duration - $T_s$	5 ps
$a_{PPM}$ & $E_m$ pulse width - FWHM	2 ps
AND gate switching window width - $T_{sw}$	5 ps



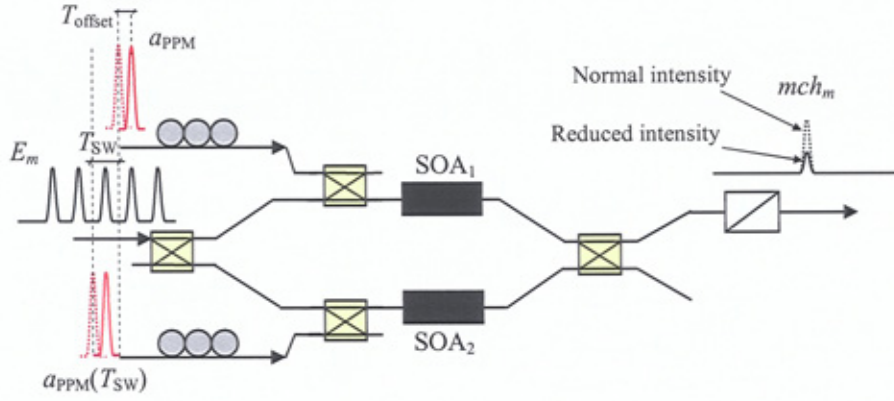
(c)

**Figure 7.11** Simulated normalised power of matching pulse  $mch(t)$  against the last switching stage inter-output contrast ratio  $CR_{OP12}$  for  $a_{PPM}$  power values of 5, 10 and 15 mW

For a low value of  $CR_{OP12}$ , unwanted pulse-power  $P_{PPM-HEM,max}$  is high (7.1), thus the matching-pulse  $mch$  power (normalised to the matching-pulse power obtained when  $CR_{OP12}$  is 0dB) is relatively high resulting in incorrect matching results at the output of AND gate, see Figure 7.10(b). However, if  $CR_{OP12}$  is relatively high, i.e.  $\geq 17.5$  dB,  $P_{PPM-HEM,max}$  is low thus the power of the unwanted matching pulse  $mch$  will be negligibly low ensuring correct operation of the PPM-HP. Note that higher power of  $a_{PPM}$  will also increase  $P_{PPM-HEM,max}$ , thus the last switching stage needs to have a higher value for  $CR_{OP12}$  in order to offset this increase for maintaining the correct operation of the PPM-HP.

### 7.3.2 Timing offset and matching gain in AND gate

The timing offset  $T_{offset}$  between  $a_{PPM}(t)$  (solid line) and the  $E_m$  input to the  $m^{th}$  SMZ-based AND gate, due to the improper timing synchronisation between PPRT and PPM-ACM, will introduce the intensity fluctuation [189, 211] in the matching pulse  $mch_m(t)$ , see Figure 7.12. In case the intensity of  $mch_m$  is too low, it is unable to control the dedicated OSWC and OSW for packet switching, thus reducing the reliability of PPM-HP. For  $T_{offset} = 0$ , a pulse, from the entry stream  $E_m$  is switched to generate a matching pulse  $mch_m(t)$  with a high intensity when  $a_{PPM}(t)$  (dashed line) is applied. However, if  $T_{offset} \neq 0$ , the matching pulse  $mch_m$  intensity is reduced because of the SMZ non-rectangular SW profile [74]. Note that, only the switched pulse intensity will change with  $T_{offset}$ , but not its time position, see Figure 7.12.



**Figure 7.12** AND gate and the timing offset between  $a_{PPM}(t)$  and PPRT entry

Figure 7.13 presents the gain of the AND gate against the timing offset (normalised by PPM-slot duration  $T_s$ ) for two values of SMZ  $T_{SW}$ . Simulation parameters are given in Table 7.6 and Table 4.2.

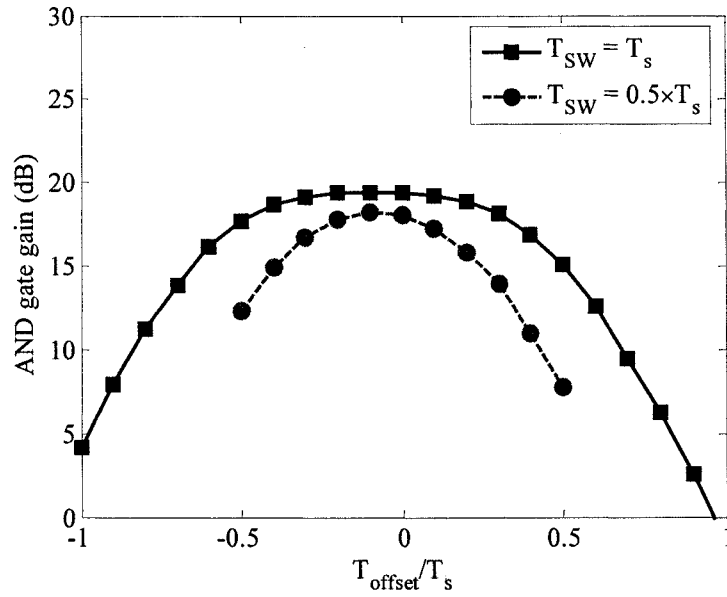
**Table 7.6** AND gate parameters for timing offset against matching gain simulation

Parameters	Values
Power of $a_{PPM}$	11.7 dBm (15 mW)
Power of PPRT entry - $P_{E-m}$	0 dBm (1 mW)
PPM slot duration - $T_s$	5 ps
$a_{PPM}$ & $E_m$ pulse width - FWHM	2 ps

A non-zero  $T_{offset}$  will penalise the AND gate gain. It is shown that, when  $T_{offset}$  is large (i.e.  $\sim T_s$ ), the AND gate gain is significantly reduced. For  $T_{SW} = T_s = 5$  ps, the achieved gain is higher than for  $T_{SW} = 0.5 \times T_s$ , since the SW gain is higher (see Figure 3.11). In addition a large  $T_{SW}$  will improve the AND gate immunity to a larger timing offset, but at the cost of increased PPM slot duration  $T_s$ , thus requiring longer PM-HP processing



time. In this work, the  $T_{SW}$  of the AND gate is set equal to  $T_s$ . Thus, from Figure 7.13, the achieved maximum gain of the AND gate is 19 dB over a range of  $\pm 0.2$  of normalised  $T_{offset}$ , dropping rapidly for higher values of normalised  $T_{offset}$ .



**Figure 7.13** The gain of the AND gate output (in matching condition) against the normalised timing offset (by  $T_s$ ) for a range of  $(-1,1)$

Note that in the optical system there will also be timing jitter associated with the optical transmitter and long-haul transmission which randomly alter the bit positions of the packet bits (clock, address and data) in the order of sub-picosecond-RMS variance [188]. However, in the proposed PPM-HP router, the PPM-ACM is designed to use only the states (0 or 1) of the address bits to set the on/off states for  $1 \times 2$  switches over a much longer duration, in the order of hundreds of picoseconds (Sections 5.4.1 and 6.3).

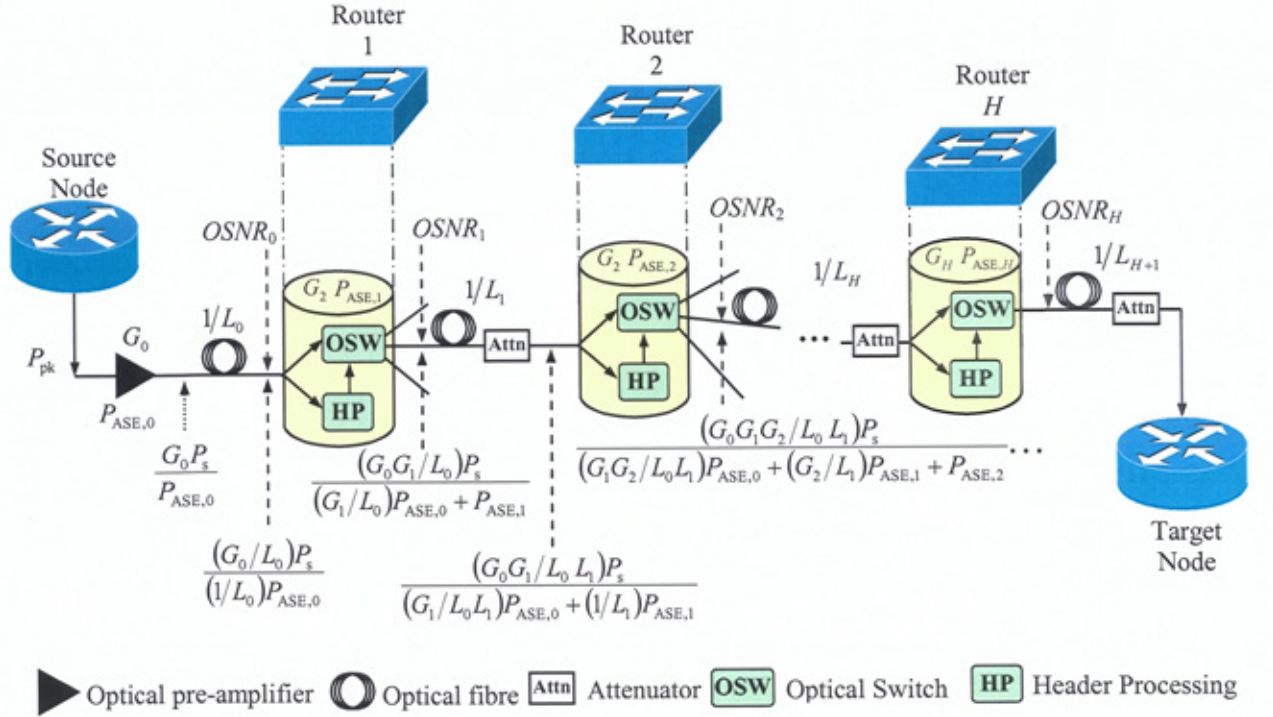
Thus the transmitter and long-haul transmission jitters are negligible in terms of the timing offset appearing in  $a_{\text{PPM}}$  and  $E_m$ .

## **7.4 Multiple-Hop Routing Performance**

In a packet switching network, data packets are typically switched through a number of intermediate routers (nodes) before arriving at the destination, thus affecting the quality of the received packets. This section examines the main factors that contribute to degradation of the routed signal quality measured, in terms of the accumulated OSNR and data-control crosstalk.

### **7.4.1 Optical signal-to-noise-ratio**

Noise in routing is characterised by the switching noise induced by the individual OSW provided that the control and input data signals are fully separable at the OSW output (i.e. orthogonally polarised). In the multiple-hop routing scenario, noise is accumulated when a packet is switched through a number of routers. Figure 7.14 presents the signal and ASE noise propagation in  $H$  hops from a source edge node to a target edge node.



**Figure 7.14** Diagram of a multiple-hop routing path from a source node, via  $H$  core PPM-HP routers (nodes), to a target node. Signal and ASE noise power are accumulated during the multiple-hop propagation

The data packet shown in Figure 7.14 with a pulse peak power  $P_{pk}$  is transmitted from a source edge node to a target edge node via  $H$  core routers. The data packet is pre-amplified and passed through a fibre span before being applied to the first router. The unpolarised ASE noise power given in (6.10) adopted for the pre-amplifier and OSW is given as:

$$P_{ASE,i} = 2n_{sp,i} h f_0 (G_i - 1) B_o \quad i = 0, 1, \dots, H \quad (7.2)$$

where  $n_{sp,i}$  and  $G_i$  are the spontaneous-emission factor and the gain of the amplifier, respectively, where  $i = 0$  represents the pre-amplifier and  $i > 0$  denotes the  $i^{\text{th}}$  OSW

module. The theoretical prediction of the OSNR at the output of the  $H^{\text{th}}$  router is computed by [5, 84, 212]:

$$OSNR_H = \frac{\left( G_H \prod_{h=0}^{H-1} (G_h / L_h) \right) P_{\text{pk}}}{\sum_{h=0}^{H-1} \left( P_{\text{ASE},h} \prod_{k=h+1}^H (G_k / L_{k-1}) \right) + P_{\text{ASE},H}} \quad (7.3)$$

where  $L_h$  is the total loss incurred from the output of the  $(h - 1)^{\text{th}}$  router to the input of the  $h^{\text{th}}$  router.

Figure 7.15 illustrates the predicted and simulated OSNR against the number of hops for a range of  $OSNR_0$ . Simulation parameters are given in Table 7.2 and Table 4.2. From theoretical calculation (using equation (7.3)), the switched packets are assumed to have the same power. However in practice, packets with different starting patterns experience magnitude fluctuations which increase with the number of hops thus resulting in packet power variations. This effect is illustrated in Figure 7.15, where, for a lower number of hops (i.e.  $\leq 3$ ), there is a good agreement between the predicted and simulated OSNR results. Whereas for a higher number of hops the simulated results are lower than the predicted data, e.g. for 5 hops, the difference is 4 dB. It is noted that the required OSNR is 20 dB for correct optical system operation [5]. Increasing  $OSNR_0$  has very little effect on the OSNR at higher values of hops. This is because  $P_{\text{ASE},0} < P_{\text{ASE},h}$ , and the hop gain is set at unity. Employing an optical filter with reduced bandwidth will result in reduced ASE power. However, the gain in ASE reduction is offset by the inter-symbol

interference (ISI) due to pulse spreading at high-speed packet transmission when the filter bandwidth is limited.

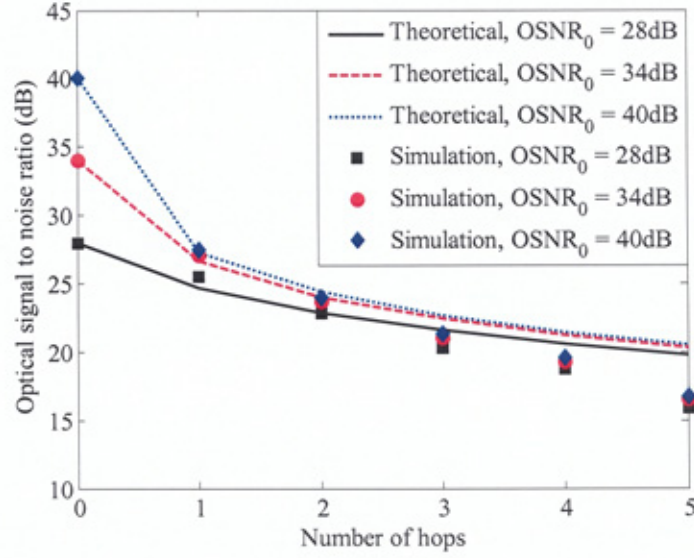


Figure 7.15 OSNR at each router output against the number of PPM-HP routing hops

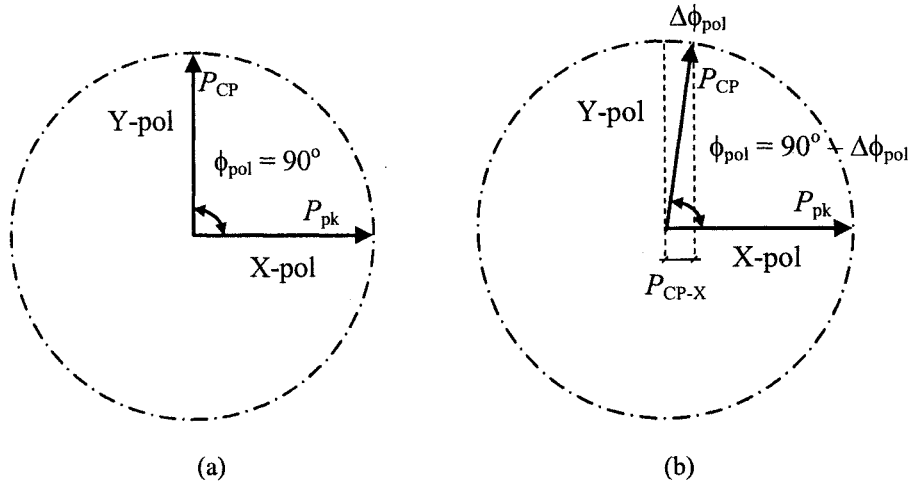
#### 7.4.2 Multiple-hop routing crosstalk performance

By placing a guard band between two transmitted packets and employing SMZ's with high  $CR_{CH1}$  ( $\sim 25$  dB, see Figure 4.8), the SMZ's  $RCXT$  would be negligible in comparison to the data-control crosstalk  $CXT_{D-CP}$  discussed in Section 6.6.3. The latter, caused by the imperfect separation of data and control signals, would be considerable, since the control signal power is typically larger than the data signal power. In this work, control and data signals have been differentiated between using orthogonal polarisation ( $\phi_{pol} = 90^\circ$ ), see Figure 7.16(a). Data and control signals are set in the X and Y polarisations, respectively. Assuming that the control pulse polarisation is offset by a

$\Delta\phi_{\text{pol}}$  in Figure 7.16(b) and the control pulse power is  $P_{\text{CP}}$ , the amount of control power projected to X-polarisation  $P_{\text{CP-X}}$  distorting the desired switched signal, is computed by

$$P_{\text{CP-X}}(\text{dB}) = 10 \log_{10} [P_{\text{CP}} \times \cos(90^\circ - \Delta\phi_{\text{pol}})] + G_{\text{SOA-CP}}(\text{dB}) - 6(\text{dB}), \quad (7.4)$$

where  $G_{\text{SOA-CP}}$  is the SOA amplification gain on a CP. The 6 dB loss is due to the control and output couplers of the SMZ.



**Figure 7.16** (a) Perfect orthogonal-polarisation separation with  $\phi_{\text{pol}} = 90^\circ$ , and (b) showing polarisation offset  $\Delta\phi_{\text{pol}}$

Therefore, the data-control crosstalk, computed by the ratio between the undesired control signals leaked to the X-pol and the switched data packet at the router output, is given by:

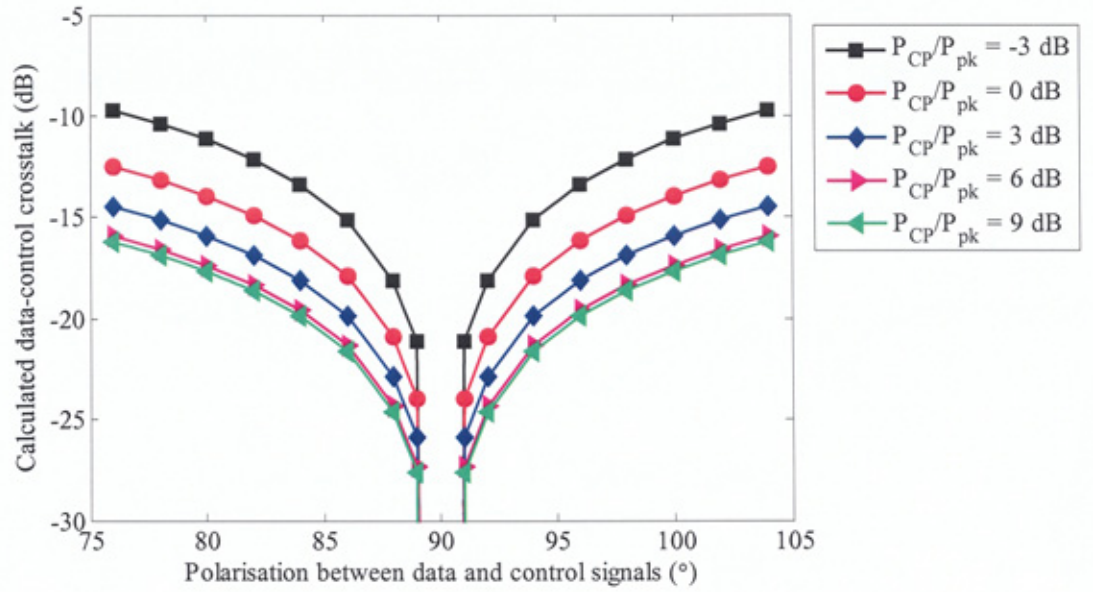
$$CXT_{\text{D-CP}} = 10 \log_{10} \left( \frac{P_{\text{CP-X}} \times K^L}{P_{\text{pk}} \times (0.5 \times T_{\text{pk}} \times T_{\text{b}}^{-1})} \right), \quad (7.5)$$

with an assumption that both control and data signals receive the same OSW gain (i.e. SOA gain).  $K^L$  and  $(0.5 \times T_{pk}/T_b)$  are the numbers of control and data packet pulses (assuming that the probabilities of transmitted bits “0” and “1” are 0.5), respectively. In (7.4) it is shown that  $P_{CP-X}$  is symmetrical for both positive and negative values of  $\Delta\phi_{pol}$ , leading to symmetry in  $CXT_{D-CP}$  (7.5) respect to  $\Delta\phi_{pol}$ . Figure 7.17(a) and (b) show the calculated (7.5) and simulated data-control crosstalk  $CXT_{D-CP}$  plotted against the polarisation  $\phi_{pol}$ , respectively, for a range of  $P_{CP}$  (normalised by  $P_{pk}$ ). The predicted and simulation parameters are given in Table 7.7.

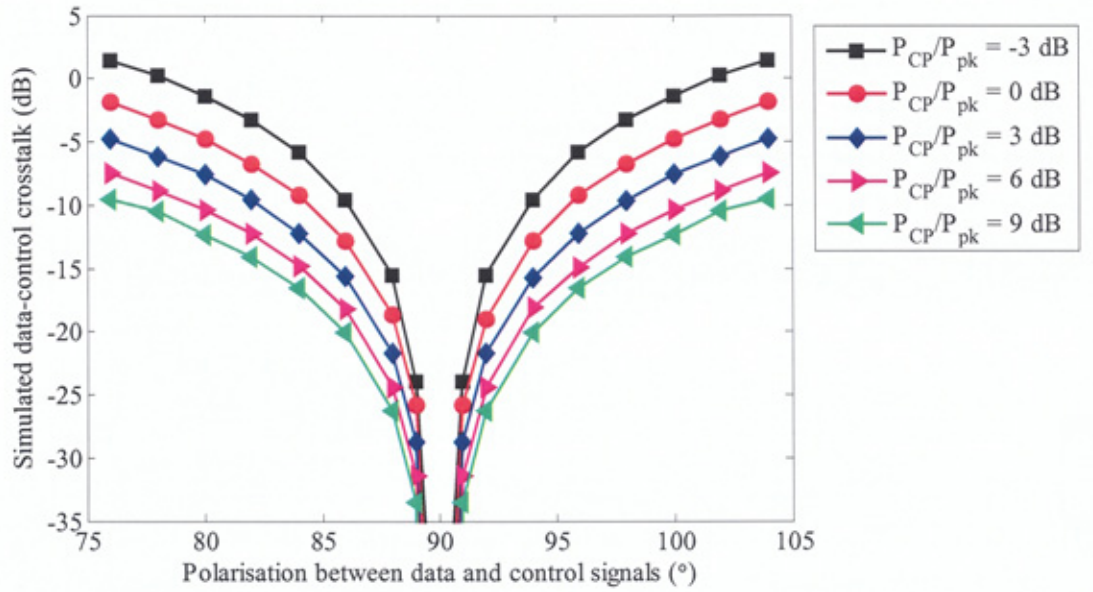
**Table 7.7** Multiple-hop routing parameters for data-signal crosstalk simulation

Parameters	Values
Input data bit rate	100 Gbit/s
Data packet length	64 bytes (512 bits)
Optical wavelength - $\lambda_0$ (equivalent to optical frequency - $f_0$ )	1554 nm (193.05 THz)
Data & CP width - FWHM	2 ps
PPM slot duration - $T_s$	5 ps
Packet duration - $T_{pk}$	5.17 ns
Data pulse (peak) power - $P_{pk}$	1.45 dBm (1.4 mW)
Range of $P_{CP}/P_{pk}$	0, 3, 6, 9 dB
Optical bandwidth - $B_o$	300 GHz
Number of CPs for OSW ( $K^L$ )	64 ( $K = L = 4$ )
Number of routing hop	5
Net gain (in multiple-hop routing)	0 dB





(a)



(b)

**Figure 7.17** Data-control crosstalk induced against the polarisation between data and control signals in individual PPM-HP router for a range of normalised  $P_{CP}/P_{pk}$ : (a) calculated and (b) simulated crosstalk



In both graphs it is shown that minimum crosstalk is achieved at orthogonal polarisations of data and control.  $CXT_{D-CP}$  increases when orthogonality no longer exists. Higher  $P_{CP}$  will create a greater SW gain, thus increasing the switched packet power and hence increased  $CXT_{D-CP}$ . However, if  $P_{CP}$  is high, it would saturate the SOA, resulting in a small improvement in  $CXT_{D-CP}$  (see  $P_{CP}/P_{pk}$  of 6 dB and 9 dB in Figure 7.17(a) and (b)). The obtained simulation results differ from the predicted ones within a range of a few dB, when  $\Delta\phi_{pol} < 5^\circ$ . However, the difference is larger for greater  $\Delta\phi_{pol}$ . This is due to the OSW gain, which is assumed to be identical, for both the control and data signals for theoretical calculation simplicity. However, this assumption is not valid for the simulation because the crosstalk measurements are carried out by measuring the switched data power in the orthogonal polarisation condition and then the leaked power at the OSW output when the CP is applied with  $\Delta\phi_{pol} \neq 0$ . Therefore, a greater value of  $\Delta\phi_{pol}$  leads to a larger  $P_{CP-X}$ , which in turn greatly amplifies  $P_{CP-X}$  compared to the case for smaller values of  $\Delta\phi_{pol}$ .

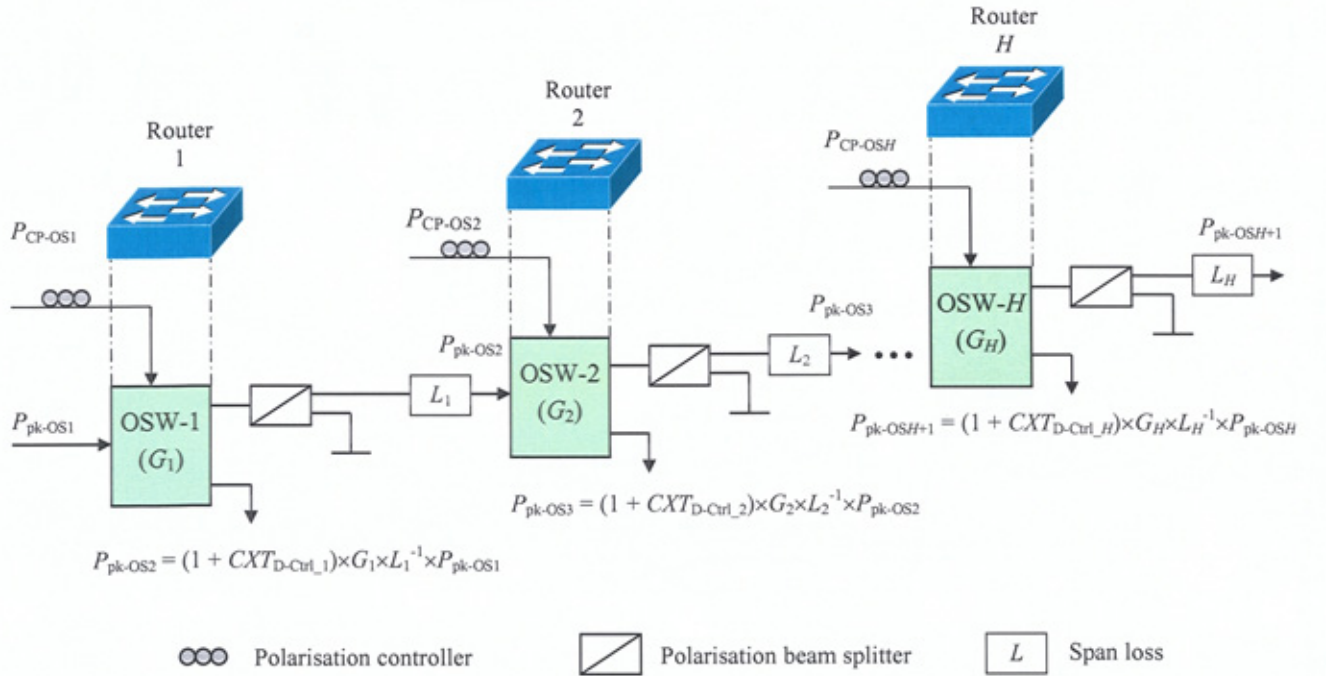
In multiple-hop routing, the  $P_{CP-X}$  will propagate together with the switched packets via multiple routers without being separated. In addition, intermediate routers will add their own  $P_{CP-X}$  to the switched signal, thus further degrading the  $CXT_{D-CP}$ . It is therefore desirable to estimate the accumulated  $CXT_{D-CP}$ . Figure 7.18 illustrates the propagation of signal and crosstalk through a routing path including  $H$  routers. The relationship between an  $H$ -hop routed signal ( $P_{pk-OSH+1}$ ) and the input signal ( $P_{pk}$ ) is expressed by:

$$P_{pk-OSH+1} = (1 + CXT_{D-CP, tot-H}) \times P_{pk}, \quad (7.6)$$

where  $CXT_{D-CP,tot-H}$  is the total (accumulated) crosstalk after router  $H$ . Assuming that the net gain of each router and the fibre span is unity, i.e.  $G_h/L_h = 1$ ,  $CXT_{D-CP,tot-H}$  is calculated by:

$$CXT_{D-CP,tot-H} = \prod_{h=1}^H (1 + CXT_{D-CP\_h}) - 1, \quad (7.7)$$

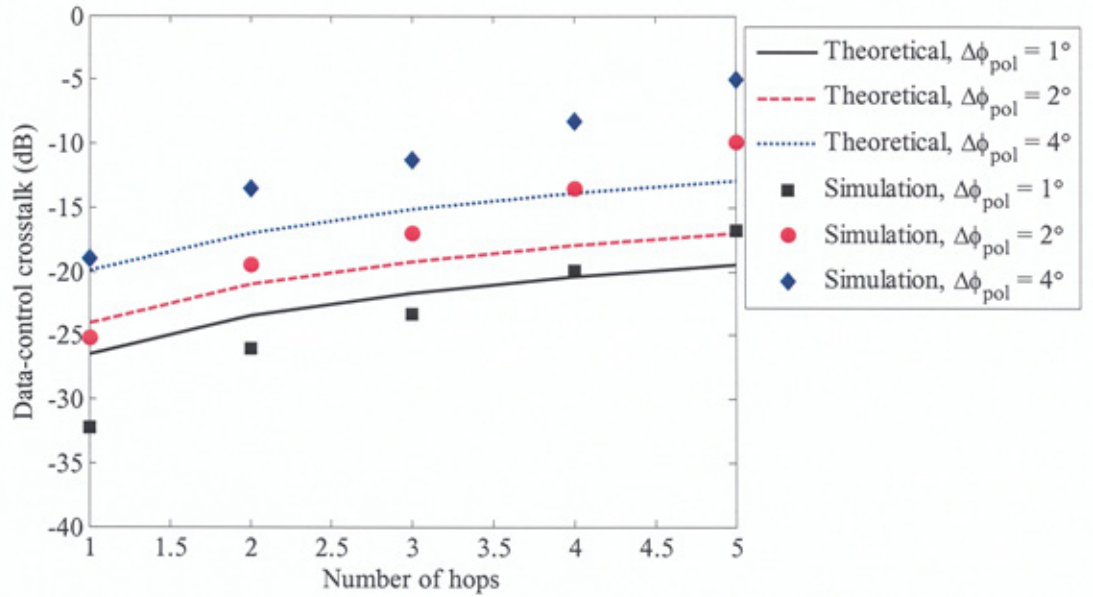
where  $CXT_{D-CP\_h}$  is the data-control crosstalk at router  $h$ .



**Figure 7.18** Diagram of a multiple-hop routing path including  $H$  core PPM-HP routers (nodes). Data-signal crosstalk is accumulated during the multiple-hop propagation

Predicted and simulated  $CXT_{D-CP}$  performances against the number of hops for a range of  $\Delta\phi_{pol}$  are depicted in Figure 7.19 with the parameters previously given in Table 7.7. In theoretical evaluation, values of data-control crosstalk in all routers are assumed to be identical. Both predicted and simulated results show an increase in  $CXT_{D-CP}$  with the

number of hops for all values of  $\Delta\phi_{\text{pol}}$ . For a low value of  $\Delta\phi_{\text{pol}}$  ( $1^\circ$ ), the  $CXT_{\text{D-CP}}$  is around 20 dB (for both theoretical and simulated results) after a packet is switched via five routers. A further increase in  $\Delta\phi_{\text{pol}}$  induces a greater multiple-hop routing crosstalk penalty, which in turn limits the number of hops. The divergence between theoretical and simulated results is due to the assumption that the OSW gain and  $CXT_{\text{D-CP}}$  are identical at all routers for calculation. The OSW gains in simulation, however, are varied due to the different input power at each router when crosstalk is presented (instead of a constant  $P_{\text{pk}} = 1.4$  mW). Additionally, the crosstalk value at each router would also be varied for different input power (see Figure 7.17).



**Figure 7.19** Calculated and simulated data-signal crosstalk against the number of routing hops for  $\Delta\phi_{\text{pol}}$  values of  $1^\circ$ ,  $2^\circ$  and  $4^\circ$

## 7.5 Router Features

This section discusses the router features including the header recognition time and the input/output characterisation. In conclusion, it will summarise the main router specifications.

### 7.5.1 Header recognition time

Header recognition includes the PPM-address conversion (in PPM-ACM) and correlation times between  $a_{\text{PPM}}$  and a PPRT entry (to the AND gate). Since both tasks could be carried out simultaneously, the header recognition time due to PPM-HP  $T_{\text{PPM-HP}}$ , see Figure 5.2, is determined by the duration of a  $2^N$ -slot PPM-frame as:

$$T_{\text{PPM-HP}} = 2^N \times T_s. \quad (7.8)$$

Note that  $M$  AND gates are used to correlate  $a_{\text{PPM}}$  with  $M$  PPRT entries in parallel. In a conventional header recognition scheme using the exhaustive (brute-force) correlation algorithm employing  $M$  AND gates, the required header recognition time  $T_{\text{EX-HP}}$  is:

$$T_{\text{EX-HP}} = 2^N \times N \times T_{\text{AND}} \times M^{-1}, \quad (7.9)$$

where  $T_{\text{AND}}$  is the minimum time interval required for the gains of the AND gates to recover between two successive AND operations (i.e. the SOA recovery time). Typically  $T_{\text{AND}}$  (hundreds of picoseconds) is much greater than  $T_b$  (few picoseconds) in multi-hundred Gbit/s optical networks. The header recognition time gain,  $R_T$ , is defined

as the ratio of the time required for the brute-force approach  $T_{\text{EX-HP}}$  over the required time for PPM-HP  $T_{\text{PPM-HP}}$ , and is given by:

$$R_T = \frac{N \times T_{\text{AND}}}{M \times T_s}. \quad (7.10)$$

### 7.5.2 Input-output power range

The dynamic operation range of the proposed PPM-HP router gain plotted against the input power, i.e. received power (peak pulse power), is presented in Figure 7.20.

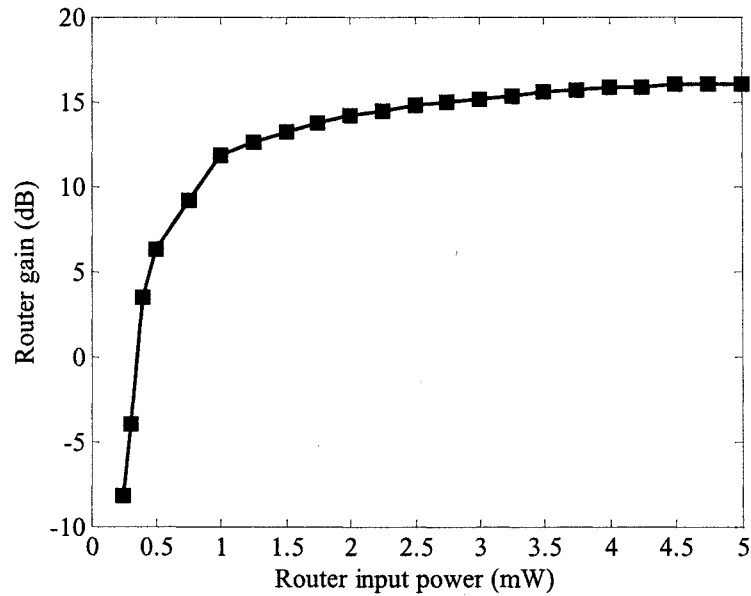


Figure 7.20 PPM-HP router gain against the input (packet) power

The router gain is relatively low ( $< 10$  dB) when the input power is small ( $P_{\text{pk}} < 0.75$  mW). This could be explained by the overall underperformance gains of the CEM, SPC,

PPM-ACM, AND gate and OSW when the applied signals have a low power. The router gain is saturated, and shows a small increase with input power since high input power will saturate the gains of the CEM and OSW, so the switched signal power is relatively constant.

In this work, the theoretical calculation and simulation investigations were carried out at the selected input power of 1.4 mW (i.e. input-power operation point), where the router gain is sufficiently high for amplification of the switched packet before being transmitted via the next fibre span. The minimum required power of the router (i.e. router sensitivity) is set at the minimum input power level where the router gain is 0 dB. From Figure 7.20, the router sensitivity is 0.45 mW (-3.5 dBm).

### 7.5.3 Router specifications

PPM-HP router specifications are summarised in Table 7.8:

**Table 7.8** PPM-HP router specifications

SPECIFICATIONS	VALUES
Operation wavelength	1554 nm
Operation bit rate	100 Gbit/s
Maximum bit rate (need to reconfigure the variable switch window widths in CEM and SPC)	200 Gbit/s (as PPM slot duration $T_s = 5$ ps)
Number of address-bit processing (upgradeable by adding more switching stage in PPM-HEM)	4 bits
Operation gain	12.5 dB
Saturation gain	16 dB
Sensitivity	- 3.5 dBm
Noise figure	6 dB
DC current bias	0.15 A
Temperature	300 °K
Maximum number routing hops	4
Broadcast capability	Yes
Multicast capability	Yes
Maximum of routing hops (based on data-control crosstalk)	5 ( $\Delta\phi_{pol} = 1^\circ$ )
	3 ( $\Delta\phi_{pol} = 2^\circ$ )
	1 ( $\Delta\phi_{pol} = 4^\circ$ )
Optical filter bandwidth	300 GHz

## 7.6 Summary

Chapter 7 has presented the operation and performance investigation of the proposed PPM-HP routers. The chapter began with VPI simulations of single and multiple wavelength routers for single and multiple hop routing which validated the PPM-HP concept. The reliability of PPM-HP was next investigated through the study of the resultant matching pulse power achieved in the presence of the low inter-output contrast ratio of switches in PPM-ACM. It was shown that, in PPM-ACM, the  $1 \times 2$  switch inter-output  $CR_{OP12}$  is required to be larger than 17.5 dB to limit the incorrect matching pulse power. In addition the reduced AND-gate gain, due to the timing offset between the converted PPM-address and the PPRT entry, has been plotted, which determines the timing offset tolerance in PPM-HP. In order to investigate the noise and data-control crosstalk characteristics of the router, it was found to be best to explore the router in multiple-hop routing scenarios. From this, the maximum number of routing hops was also obtained at four hops, for a target OSNR of 20 dB. Single router and multiple-hop routing  $CXT_{D-CP}$  have been investigated, showing the penalty in crosstalk of imperfect data and control separation. Header recognition time and the input/output power characteristic were examined, and the router operation specifications were summarised. Finally, the limitations of the PPM-HP router were specified.

Papers [A9], [A11], [A19] and [A22] presented the results of the single-wavelength PPM-HP router in which [A11] demonstrated the multiple hop routing and associated noise accumulation. The multiple-wavelength router results were published in [A12] and [A14]. The timing offset concept and investigation can be found in paper [A9]. The



data-control crosstalk performance is under preparation for publication and will be available in due course.

## **CHAPTER 8**

### **CONCLUSIONS AND FUTURE WORK**

This chapter summarises all of the important findings in the proposed PPM-HP router and ultrafast optical switches and discusses the outcomes gained throughout this research. The outlook of extending work from this research will be pointed out and discussed. Finally key remarks will conclude the thesis.

#### **8.1 Conclusions**

All-optical processing and switching are the vital building blocks in the design of an all-optical router for today and future high-speed photonic packet switching networks. Therefore, the research objectives were to address and investigate the issues in existing routing schemes, including header recognition techniques and optical switches. The primary objectives of the work were to propose a new routing scheme based on the reduced-size pulse position routing table (PPRT), to design, and to characterise a complete router based on a PPRT and evaluate the router performance in single and

multiple hop routing. In addition, the aims of the research was to improve the performance of the MZ-based ultrafast optical switches (TOAD, SMZ) for use in the proposed router as the building blocks, and to introduce a number of MZ-based switch variants (TaMZ, CSMZ and 1×2 two-SMZ switches) which offer better performance and reduced complexity in high-speed switching and demultiplexing compared to SMZ switches.

The thesis began with a comprehensive literature review of routing and switching in concurrent high-speed photonic packet switching networks, where all the router elements were designed to operate in the optical domain, in order to achieve a high routing throughput. Three main issues were identified as follows: (i) the exponential increase in the number of entries in a look-up routing table in an increased-size network, resulting in a long header processing time, (ii) the correlation speed limitation due to the long recovery time of AND, OR, XOR gates based on SOAs, in comparison to the high bit-rate data packet, which affects the speed and complexity of header processing and (iii) the limited scalability in upgrading the routing table that requires additional hardware and increased processing time.

Comprehensive reviews of ultrafast optical switches were given and their advantages and drawbacks were identified. In particular the narrow and symmetrical switching window profile was highlighted as a crucial feature of an ultrafast optical switch with low residual crosstalk for use as a building block in an all-optical router.

The switches were investigated in Chapters 3 and 4. Exploitation of the SOA nonlinear properties in the design of ultrafast optical switching (XGM, XPM and FWM) were discussed and the fundamentals of the TOAD switch based on an optical loop interferometer were briefly introduced. A dual-control pulse scheme was introduced for the TOAD switch, resulting in a reduced residual crosstalk in switching and demultiplexing of around 10 dB. The bit error rate performance was evaluated, and it was shown that there was additional  $\sim 1$  dB gain in power penalty compared with the conventional single control pulse based switches.

On the basis of the SOA and optical interferometer understanding, an improved SMZ switch, new Tri-arm Mach-Zehnder and chained symmetric Mach-Zehnder switches were introduced in Chapter 4. The SMZ residual crosstalk and the proposal of an unequal control-pulse scheme for crosstalk suppression were first presented. The on/off inter-output and inter-channel contrast ratios, important factors in the restraint of the multiple pulse effect in the serial connection of  $1 \times 2$  switches used in the PPM address conversion module, were investigated. The proposed TaMZ would help to improve switching contrast ratios by using two high contrast-ratio outputs of two common-arm SMZs as TaMZ outputs. For the TaMZ switch, high inter-channel and inter-output contrast ratios of 25 dB and 20 dB, respectively, were observed at its outputs. The tri-arm MZ architecture was further extended to a multiple-arm MZ, resulting in a  $1 \times M$  CSMZ switch, offering  $M$ -channel OTDM demultiplexing with 50% reduction in the number of SOAs, in comparison to the multiple SMZs. Performance investigations, including interferometer stability against the switching contrast ratio and power penalty,

were presented to evaluate the proposed TaMZ and CSMZ, respectively. It was shown that the TaMZ switching contrast ratios were varied over a range of a few dB when the input/output coupling ratios  $\alpha \neq 0.5$ . In CSMZ, the received power penalty is greatly dependent on the data channel being demultiplexed, when  $\alpha \neq 0.5$ . For even channels, a higher power penalty is observed when  $\alpha > 0.5$ , in comparison to the case for  $\alpha < 0.5$ , whereas the opposite is true for the odd channels. In addition, the calculation and simulation data confirmed that the offset of  $\alpha$  from 0.5 in the output couplers will much affect the TaMZ and CSMZ arm balance (i.e. stability), thus resulting in lower contrast ratios and higher power penalty, respectively, in comparison to the input couplers.

The concept of reducing the size of the look-up routing table in packet switching routers was introduced in Chapter 5. It was shown that the size of the routing table is reduced from  $2^N$  to  $M$  when employing a new routing table entry in PPM format in comparison to the existing tables. In the proposed PPRT, the total number of entries is fixed, and equal to the number of router output ports, regardless of the packet header address bit length  $N$  and the network size. PPRT configuration makes packet header address correlation rather simple, since it only requires a single bit-wise AND gate, resulting in reduced complexity and processing time. Architectures for single and multiple-wavelength PPM-HP routers, based on the PPRT, were proposed and modelled.

In Chapter 6, key modules for the PPM-HP router were discussed and studied in detail. The synchronisation issue (i.e. clock extraction) was reviewed, and a new two-inline SMZ based clock extraction module was proposed, offering a fast response time, a

simple architecture, and high contrast ratio of 20 dB, for a given control pulse power. The pulse-position-modulation header extraction module (PPM-HEM), consisting of a serial-to-parallel packet address converter and PPM address conversion, was introduced. In this, a newly proposed  $1 \times 2$  high contrast ratio switch, using two SMZs, offered similar contrast ratios to that of TaMZ, but with reduced complexity, was implemented. It was shown that, in PPM-HEM, both the contrast ratio and multiple pulse effect were dependent on the inter-output contrast ratio of the  $1 \times 2$  switch and the size of the PPM address conversion (i.e. input arrival delay parameter). A longer header address (i.e. large  $N$ ) would require a higher power for the PPRT input pulse due to the coupler/splitter losses. A bank of ultrafast optical AND gates based on SMZs were adopted as the correlator. Only one bitwise correlation was needed to compare fully the PPM address with all slots in each PPRT entry, thus overcoming the gain recovery issue associated with AND gates based on SOAs.

The router optical switch played a crucial role in routing performance in terms of speed, accumulated noise and crosstalk. A  $1 \times M$  switch was presented including multiple SMZs, to ensure an ultrafast switching response (of the order of picoseconds). Relatively constant switching gain was maintained by employing a control signal with a constant power or multiple pulses to overcome the fast relaxation of the SOA carrier density of hundreds of picoseconds (i.e. gain recovery), compared with a long packet with its temporal length of nanoseconds. The ultrafast all-optical flip-flop (AOFF) and multiple-pulse generator were introduced to generate the control signals for wavelength conversion and OSW in the WDM and single-wavelength PPM-HP router, respectively.

The AOFF could operate regardless of the actual feedback loop delay using multiple set/reset signals. The noise induced by each router output was determined, based on the calculation of the amplified spontaneous emission (ASE) noise source of SOAs.

Simulations were carried out to verify the operations of the proposed single and multiple-wavelength PPM-HP routers. The accumulated noise and data-control crosstalk in the multiple-hop routing scenario was analytically modelled and compared with the simulation data in Chapter 7. It was shown that, without forward error control (FEC) and signal regeneration (2R or 3R), the number of routing hops is limited to four when a target received OSNR is 20 dB. The router input/output power was characterised, showing that the minimum required input power for the router (i.e. router sensitivity) to be -3.5 dBm.

In conclusion, a novel all-optical packet switching router, based on the PPM-HP has been proposed and investigated. It has been shown to reduce considerably the routing table size, to overcome the SOA gain recovery issue, thus offering robustness in high-speed all-optical header processing. The PPM-HP router and its performance have been analytically characterised and analysed by means of theoretical calculation and simulation verification. In addition, new controlling schemes were proposed for the TOAD and SMZ switches, in order to improve the switching and demultiplexing residual crosstalk. The research work further extended the SMZ architecture into the TaMZ and CSMZ, to achieve an improved contrast ratio in switching and reduced

complexity in multiple-channel OTDM demultiplexing, respectively, which have led to the successful completion of the initial research aims and objectives.

## **8.2 Further Work and Outlook**

The proposed PPM-HP router presents a perspective in downsizing considerably the number of entries in a look-up routing table in today's optical packet switching networks. In this section, the potential of the PPM-HP router, and its further extension, will be discussed.

### **8.2.1 Further work**

The research work presented in this thesis focused primarily on a single-input-multiple-output PPM-HP router operating at a single wavelength. It is therefore necessary to extend the PPM router's capability to a multiple-input-multiple-output packet switching router in a WDM network. A single-input-multiple-output WDM router constructed from multiple PPM-HP modules was introduced and simulated in this work, showing the potential for fabrication of a non-blocking  $1 \times M$  WDM router. However, further work needs to be carried out on scheduling incoming packets (i.e. input buffering or optical memory) to facilitate the multiple-input-multiple-output single-wavelength and WDM routers.

A PPM-HP router could be simplified further, provided that the transmitted data packet header address is already in the PPM format. Therefore, the PPM-address is used



directly to control the AND gates, so there is no need for the PPM address conversion module. As a result, router complexity will be reduced. Further details of this scheme, and its analysis are given in paper [A9].

In addition, the PPRT concept could be extended further by the introduction of multiple  $M$ -entry PPRTs, where each entry has a much smaller length in comparison to that of the proposed PPRT. The essence of this multiple-PPRT scheme is to reduce further the processing time from  $2^N \times T_s$  to  $2^{N-K} \times T_s$  where  $K$  is the total PPRT number. Initial results of the proposed multiple PPRT scheme can be found in paper [A7].

In this work, the proposed PPRT could allocate all  $2^N$  possible address patterns for exhaustive correlation. However, in practice, it might not be necessary to search all of the routing table entries (or in other words, the router will not examine all bits of the incoming packet header address) to make a routing decision, depending on the hierarchy architecture of a network. Instead, a further intermediate router could access different subsets of a packet header address (i.e. a range of addresses) to make their own routing decisions, so the PPRT could be simplified further by the assignment of a pulse position in its entry, representing a group of addresses, such as in the all-optical IP routing scenario.

Practical implementation of the proposed PPM-HP router would be the next step forward in the verification and evaluation of the router concept. Since the router is based on the SMZ as the building block, it is therefore desirable to characterise firstly the SMZ

and its performance in an experimental test-bed. The next step is to realise clock extraction which provides seeding pulses for PPM address conversion and PPRT generation. Note that real time pulse propagation within the module components, and connections between modules, should be accounted for in order to synchronise all router modules with the arrival of an incoming packet correctly. Individual modules should be characterised experimentally. Furthermore, a practical test-bed can be built to evaluate and assess the key issues in the router including, but not limited to, multiple-hop routing latency, network throughput, scalability and the dispersion map.

### **8.2.2 Outlook**

Any future all-optical router will depend emphatically on powerful optical signal processing to cope with huge increases in data traffic in the optical fibre backbones. The technological breakthrough in the invention of the semiconductor optical amplifier in the middle of 1990's has been a driving force for the development of ultrafast optical switches and sophisticated optical data processing units, based on fundamental all-optical Boolean logic gates (AND, XOR, OR, etc.). Since then, the SOA, like the inauguration of transistors to replace transitionally vacuum tubes in the 1950's, has gradually evolved, thanks to integration and quantum technologies in recent years. It is envisaged that integrated optical circuits employing SOAs will be widely used for many processing functions in the optical domain in the coming years. In addition, the quantum-dot SOA technology proposed recently offers shorter gain recovery, thus providing a great prospect in ultrahigh speed optical processing (of the order of sub-

picoseconds) [32]. These factors would place the SOA in a centre role in optical processing, and enhance photonic router capabilities.

The emergence of optical memory is increasing in recent years, showing great interest and demands in dynamic optical routing, i.e. updating the content of look-up routing tables. Though today optical memory is complex, bulky, costly and capacity-limited, its future evolution will grow steadily, thanks to integration technology and advanced materials. As an early tryout in the optical memory area, this research work proposed an all-optical flip-flop [A3], [A10] and [A14], and extended it for the construction of an eight-bit all-optical memory with its write-in and read-out functions operated analogously to the concept of the voltage charge/discharge in a capacitor in the electrical domain. The result of this exploration is reported in paper [A6].

In summary, the router and its processing capabilities are key elements for the evolution of optical communication networks. Advanced materials and integration technologies [213, 214] will trim down the gaps of operation speed, component size and fabrication and installation cost, to realise a truly all-optical router.

## APPENDIX - A LIST OF PUBLICATIONS

### Articles and Letters in Journals

- [A1] Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "High-Speed All- Optical Time Division Multiplexed Node", *Journal of Iranian Association of Electrical and Electronics Engineers*, vol. 3, no. 2, to be appeared in 2007
- [A2] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Characterisation and Performance Analysis of a TOAD Switch Employing a Dual Control Pulse Scheme in High-speed OTDM Demultiplexer", accepted for publication in *IEEE Communications Letters*, Jan. 2007
- [A3] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "All-optical Flip-flop Based on SMZ With A Feedback-Loop and Multiple Forward Set/Reset Signals", *SPIE Optical Engineering Letters*, vol. 46, no. 4, Apr. 2007, to be appeared on Apr. 2007
- [A4] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Improvement In Received Power Penalty In OTDM System Employing All-Optical SMZ Switch With Reduced Residual Crosstalk", *The Mediterranean Journal of Electronics and Communications* (invited paper), ISSN: 1744-2400, vol. 2, no. 4, pp. 82-90, Oct. 2006
- [A5] Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "BER Performance Analysis of 100 and 200 Gbit/s All-optical Router - Demultiplexer Using Symmetric Mach-Zehnder Switch", *IEE Proceeding of Circuits, Devices and Systems* (special edition), ISSN: 1350-2409, vol. 153, no. 4, pp. 361-369, Aug. 2006

### Conference papers

- [A6] H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "High-Speed All-Optical Memory Based on Symmetric Mach-Zehnder Switches", abstract accepted for publication in the *12th European Conference on Networks & Optical Communications and Conference on Optical Cabling and Infrastructure (NOC & OCI 2007)*, Stockholm, Sweden, June 2007
- [A7] M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Ultra-Fast All-Optical Packet-Switched Router With Multiple PPM-Based Routing Table", abstract accepted for publication in the *12th European Conference on Networks*

*& Optical Communications and Conference on Optical Cabling and Infrastructure (NOC & OCI 2007)*, Stockholm, Sweden, June 2007

- [A8] H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "Simulations of All-Optical Multiple-Input AND-Gate Based on Four Wave Mixing in a Single Semiconductor Optical Amplifier", accepted for publication in the *14th IEEE International Conferences on Telecommunications 2007 (ICT-MICC 2007)*, Malaysia, May 2007
- [A9] M. F. Chiang, Z. Ghassemlooy, H. Le-Minh and W. P. Ng, "All-Optical Packet-Switched Routing Based On Pulse-Position-Modulated Header", accepted for publication in the *7th IASTED International Conferences on Wireless and Optical Communications (WOC 2007)*, Montreal, Canada, May-Jun. 2007
- [A10] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "An Ultrafast with High Contrast Ratio  $1 \times 2$  All-optical Switch Based on Tri-arm Mach-Zehnder Employing All-Optical Flip-flop", accepted for publication in *IEEE International Conference on Communications 2007 (ICC 2007)*, Glasgow, UK, Jun. 2007
- [A11] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "Multiple-hop Routing Based on the Pulse-Position-Modulation Header Processing Scheme in All-optical Ultrafast Packet Switching Network", proceeding of the *49th IEEE Global Telecommunication Conference (GLOBECOM 2006)*, ISBN: 1-4244-0357-X, pp. OPN06-3, San Francisco, USA, Nov.-Dec. 2006
- [A12] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "Simulation of All-optical Routing Employing PPM-Based Header Processing in Photonic Packet Switched Core Network", proceeding of the *First International Conference on Communications and Electronics (HUT-ICCE 2006)*, ISBN: 1-4244-0569-6, pp. ComNet-II, HaNoi, Vietnam, Oct. 2006
- [A13] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "Investigation of Control Pulse Power Effects on All-Optical SMZ Switch Performance", proceeding of the *5th International Symposium on Communication Systems, Networks and Digital Signal Processing (CSNDSP 2006)*, ISBN: 960-89282-0-6, pp. 449-453, Patras, Greece, Jul. 2006
- [A14] H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "All-Optical Packet Router Based on Multi-Wavelength PPM Header Processing", proceeding of the *11th European Conference on Networks & Optical Communications (NOC 2006)*, ISBN: 3-923613-40, pp. 360-367, Berlin, Germany, Jul. 2006
- [A15] M. F. Chiang, Z. Ghassemlooy, W. P. Ng, H. Le Minh and V. Nwanafio, "Crosstalk Investigation of an All-Optical Serial-to-Parallel Converter Based on the SMZ", proceeding of the *7th Annual Postgraduate Symposium on the*

*Convergence of Telecommunications, Networking and Broadcasting (PGNET 2006)*, ISBN: 1-9025-6013-9, pp.217-221, Liverpool, UK, Jun. 2006

- [A16] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "Ultrafast All-optical Self Clock Extraction Based on Two Inline Symmetric Mach-Zehnder Switches", proceeding of *the 8th International Conference on Transparent Optical Networks (ICTON 2006)*, ISBN: 1-4244-0235-2, vol. 4, pp. 64-67, Nottingham, UK, Jun. 2006
- [A17] H. Le-Minh, Z. Ghassemlooy, and W. P. Ng, "A Novel All-Optical N-Channel Demultiplexer Based on Chained Symmetric Mach-Zehnder-Interferometers in OTDM Network" proceeding of *the 13th International Conference on Telecommunications 2006 (ICT 2006)*, ISBN: 972-98368-4-1, Funchal, Portugal, May. 2006
- [A18] Z. Ghassemlooy, H. Le-Minh and W. P. Ng, "Investigation of Header Extraction Based on Symmetric Mach-Zehnder Switch And Pulse Position Modulation For All-Optical Packet Switched Networks" proceeding of *the 14th Iranian Conference on Electrical Engineering (ICEE 2006)*, pp. Co.2623, Tehran, Iran, May. 2006
- [A19] Z. Ghassemlooy, H. Le-Minh and W. P. Ng, "All-Optical Packet Header Processing Scheme Based on Pulse Position Modulation in Packet-Switched Networks", *IEE seminar of Optical Fibre Communications and Electronic Signal Processing*, ISBN: 0863415989, pp. 19/1, London, UK, Dec. 2005
- [A20] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Crosstalk Suppression in an All-Optical Symmetric Mach-Zehnder (SMZ) Switch by Using Control Pulses With Unequal Powers", proceeding of *International Symposium on Telecommunication 2005 (IST 2005)*, Vol. 1, pp. 265-268, Shiraz, Iran, Sep. 2005 (Best paper award)
- [A21] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Ultrafast Header Processing in All-Optical Packet Switched-Network", proceeding of *the 7th International Conference on Transparent Optical Networks 2005 (ICTON 2005)*, ISBN: 0-7803-9236-1, Vol. 2, pp. 50-53, Barcelona, Spain, Jul. 2005
- [A22] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "A Novel Node Architecture For All-Optical Packet Switched Network", proceeding of *the 10th European Conference on Networks and Optical Communications 2005 (NOC2005)*, ISBN: 0-9538863-8-7, pp. 209-216, London, UK, Jul. 2005
- [A23] H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Characterisation a Novel Dual-Control Terahertz Optical Asymmetric Demultiplexer Switch", proceeding of *Postgraduate Research Conference in Electronics, Photonics, Communications*

*and Networks, and Computing Science 2005 (PREP 2005)*, pp. 259-260, Lancaster, UK, Apr. 2005

- [A24] H. Le-Minh, Z. Ghassemlooy, W. P. Ng and R. Ngah, "TOAD Switch With Symmetric Switching Window", proceeding of *London Communications Symposium 2004 (LCS 2004)*, pp. 89-92, London, UK, Sep. 2004

### **Posters**

- M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "All-Optical Header Processing By Using Pulse Positions", Booklet of *UK GRAD Programme Yorkshire & North East Hub - Poster Competition & Networking Event*, Leeds, UK, May. 2007
- M. F. Chiang, Z. Ghassemlooy, W. P. Ng and H. Le-Minh, "Future Ultra-High speed Optical Networks: Optical Router Based on Slotted-Time-Domain Processing", Booklet of Presentations in 2006 of *Britain's Top Early-Stage Engineers on UK Engineering Research and R&D at the House of Commons* (Poster presentation for *SET for BRITAIN 2006*), pp. 14, London, UK, Dec. 2006
- H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "Ultrafast All-Optical Processing in Optical Communication Packet Switching Networks", Booklet of Presentations in 2005 of *Britain's Top Younger Engineers at the House of Commons (SET for BRITAIN 2005)*, pp. 49, London, UK, Dec. 2005
- H. Le-Minh, Z. Ghassemlooy and W. P. Ng, "All-Optical Header Processing By Using Pulse Positions", Booklet of *UK GRAD Programme Yorkshire & North East Hub - Poster Competition & Networking Event*, Leeds, UK, May. 2005

### **Submitted papers under reviewing**

- [A25] H. Le-Minh, Z. Ghassemlooy, W. P. Ng and M. F. Chiang, "Bit Error Rate Performance of Multiple-Channel OTDM Demultiplexer Employing A Chained Symmetric Mach-Zehnder Switch", *the 50th IEEE Global Telecommunication Conference (GLOBECOM 2007)*, Washington DC, USA, Nov.-Dec. 2007, submission for reviewing in Mar. 2007

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- 11F Metallurgy; metallography
- 11G Miscellaneous materials
- 11H Oils; Lubricants; hydraulic fluids
- 11I Plastics
- 11J Elastomers
- 11K Solvents; cleaners; abrasives
- 11L Wood; paper
- 11M Material degradation; corrosion; fracture mechanics

### Mathematical sciences

- 120 Mathematical sciences, general
- 12A Pure mathematics
- 12B Statistics; operations research
- 12C Applied mathematics

### Mechanical, industrial, civil and marine engineering

- 130 Mechanical, industrial, civil and marine engineering, general
- 13A Air conditioning; heating; lighting; ventilation; refrigeration
- 13B Civil engineering
- 13C Construction equipment; building materials
- 13D Containers; Packaging
- 13E Couplings; fittings; fasteners; joints
- 13F Ground transport systems
- 13G Hydraulic systems; pneumatic systems
- 13H Industrial processes; manufacturing processes
- 13I Machinery; tools
- 13J Marine engineering; offshore engineering
- 13K Pumps; filters; pipes; tubing; valves; pressure vessels
- 13L Safety engineering
- 13M Structural engineering
- 13N Building technology

### Methods and equipment

- 140 Methods and equipment, general
- 14A Cost effectiveness; cost-benefit analysis
- 14B Laboratories; test facilities; test equipment
- 14C Recording equipment
- 14D Equipment reliability; quality control
- 14E Reprographics; photographic processes

### Military sciences

- 150 Military sciences, general
- 15A Antisubmarine warfare
- 15B Chemical warfare; biological warfare
- 15C Defence
- 15D Military intelligence
- 15E Military logistics
- 15F Nuclear warfare
- 15G Military operations; military strategy; military tactics

### Missile technology

- 160 Missile technology, general
- 16A Missile launching; missile ground support
- 16B Missile trajectories
- 16C Missile warheads; missile fuses
- 16D Missiles

### Navigation, communications, detection and countermeasures

- 170 Navigation, communications, detection and countermeasures; general
- 17A Acoustic detection; sonar
- 17B Communication systems; telecommunications
- 17C Direction finding
- 17D Electronic countermeasures; acoustic countermeasures
- 17E Infrared detection; ultraviolet detection
- 17F Magnetic detection
- 17G Navigation
- 17H Optical detection
- 17I Radar detection
- 17J Seismic detection

### Ordnance

- 190 Ordnance, general
- 19A Pyrotechnics; explosives; ammunition
- 19B Bombs
- 19C Combat vehicles
- 19D Explosions; ballistics; armour
- 19E Fire control; bombing systems
- 19F Guns
- 19G Rockets
- 19H Underwater ordnance

### Physics

- 200 Physics, general
- 20A Theoretical physics
- 20B Elementary particles; high energy physics
- 20C Nuclear physics; particle accelerators
- 20D Atomic physics; molecular physics
- 20E Optics; masers; lasers
- 20F Acoustics; vibrations; noise analysis
- 20G Thermodynamics
- 20H Metrology
- 20I Fluid mechanics
- 20J Plasma physics; gas discharges
- 20K Solid-state physics
- 20N Astronomy; celestial mechanics
- 20O Astrophysics
- 20P Cosmic rays
- 20Q Astrogeology; planetary research

### Propulsion and fuels

- 210 Propulsion and fuels, general
- 21A Air-breathing engines
- 21B Combustion; ignition
- 21C Electric propulsion
- 21D Fuels
- 21E Jet turbine engines; gas turbine engines
- 21F Nuclear propulsion
- 21G Reciprocating engines
- 21H Rocket motors
- 21I Rocket propellants

### Space technology

- 220 Space technology, general
- 22A Astronautics
- 22B Manned spacecraft
- 22C Spacecraft trajectories; spacecraft re-entry
- 22D Spacecraft launching; ground support
- 22E Unmanned spacecraft; satellites
- 22F Extraterrestrial exploration